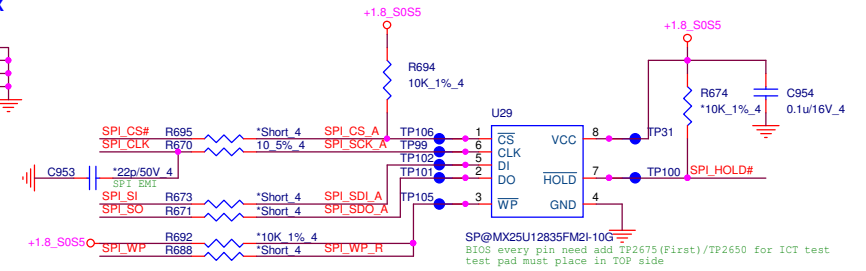




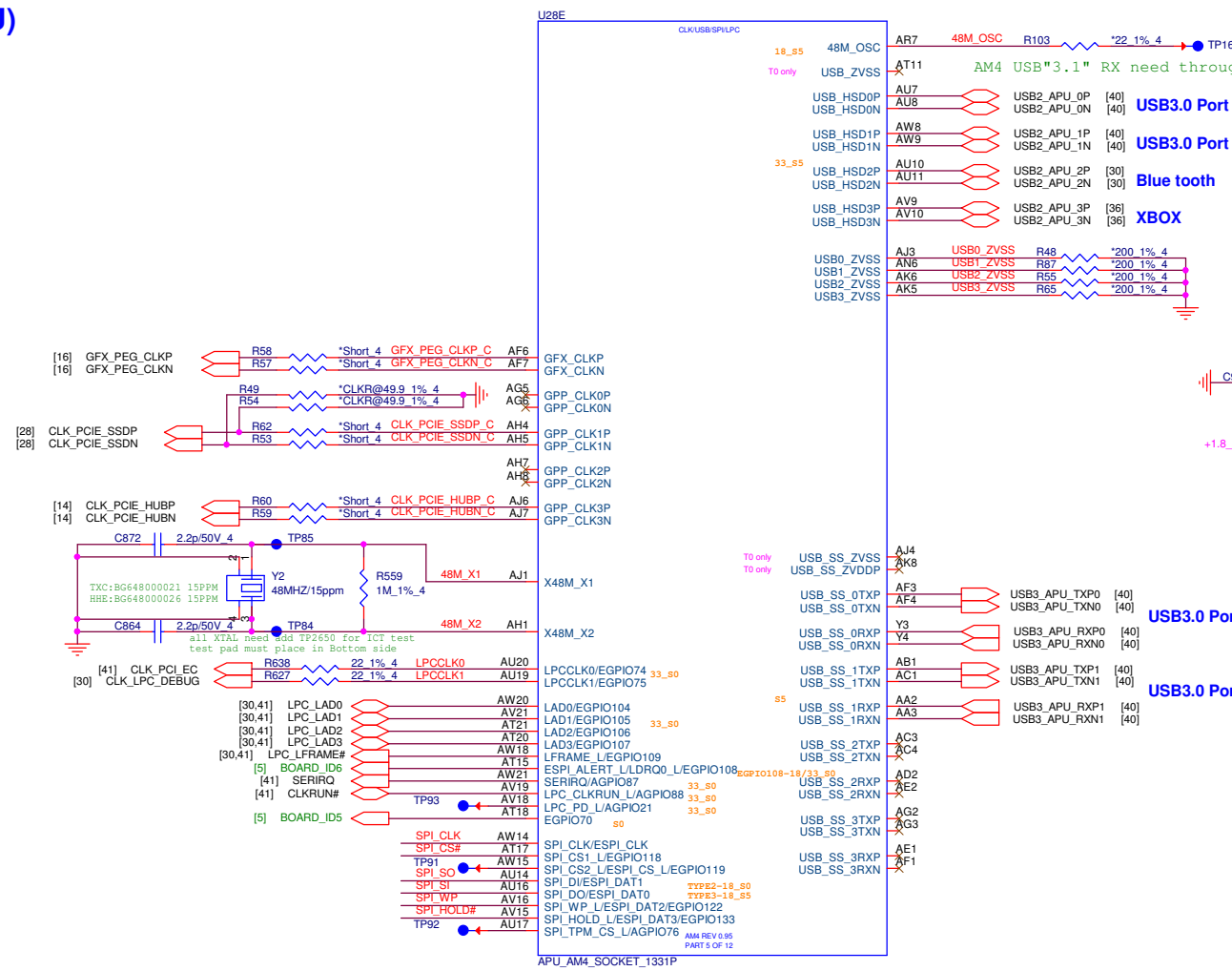


**BIOS ROM(16MB)**

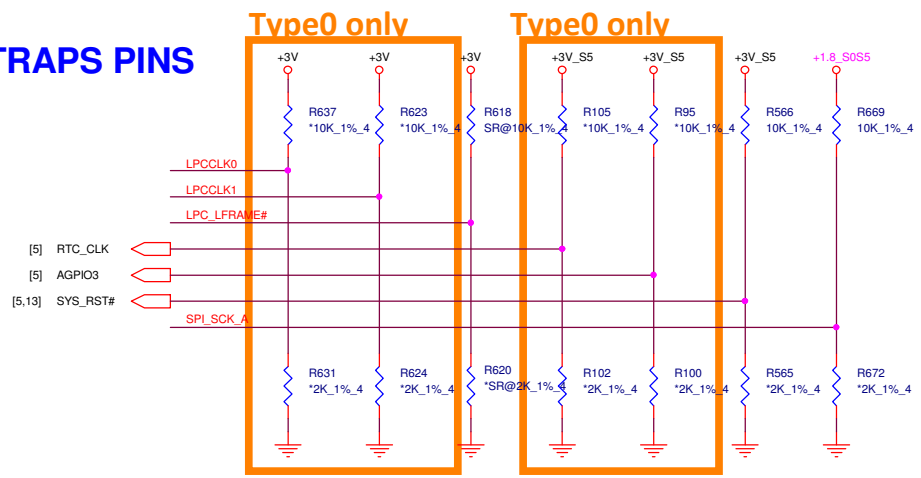


SP@ socket P/N: DG008000011 only for A-TEST  
(FP:50960-0084n-001-8p-socket)


B-STAGE need change FP to soic8-7\_9-1\_27-2\_16h



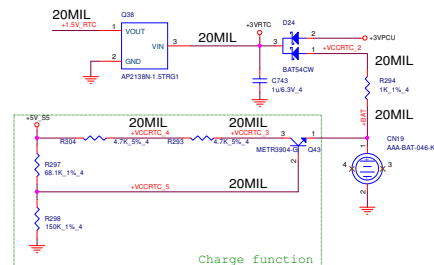
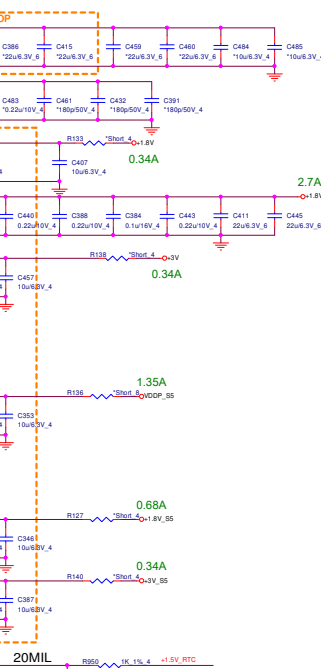
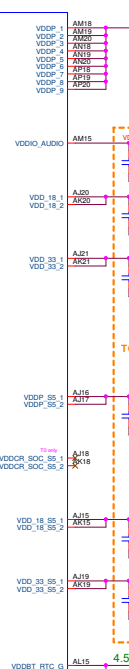
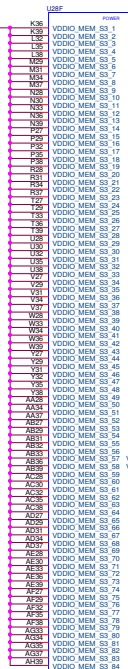
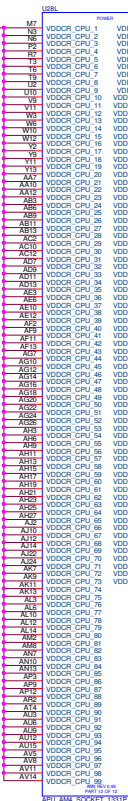
## STRAPS PINS



CZ/ST ONLY					ZP ONLY		
	LPC_CLK0	LPC_CLK1	RTC_CLK	AGPIO3	LFRAME#	SYS_RST#	SPI CLK(ZP)
PU	BOOT Fail Timer ENABLE	Use 48Mhz crystal clock and generate both internal and external clocks  DEFAULT	Coin battery is on board.  DEFAULT	Enhanced Reset logic (for quicker S5 resume)  DEFAULT	SPI ROM  DEFAULT	normal reset mode  DEFAULT	Use 48Mhz crystal clock and generate both internal and external clocks  DEFAULT
PD	BOOT Fail Timer DISABLE  DEFAULT	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	Coin battery isn't on board.	Default to traditional reset logic	LPC ROM	short reset mode	Use 100Mhz PCIE clock as reference clock and generate internal clocks only

 <b>Quanta Computer Inc.</b> <b>PROJECT : ZGX</b>			
Size	Document Number	Rev	
	<b>AM4 CLK/LPC/SPI/USB</b>	<b>1A</b>	
Date:	Tuesday, June 26, 2018	Sheet	6 of 59

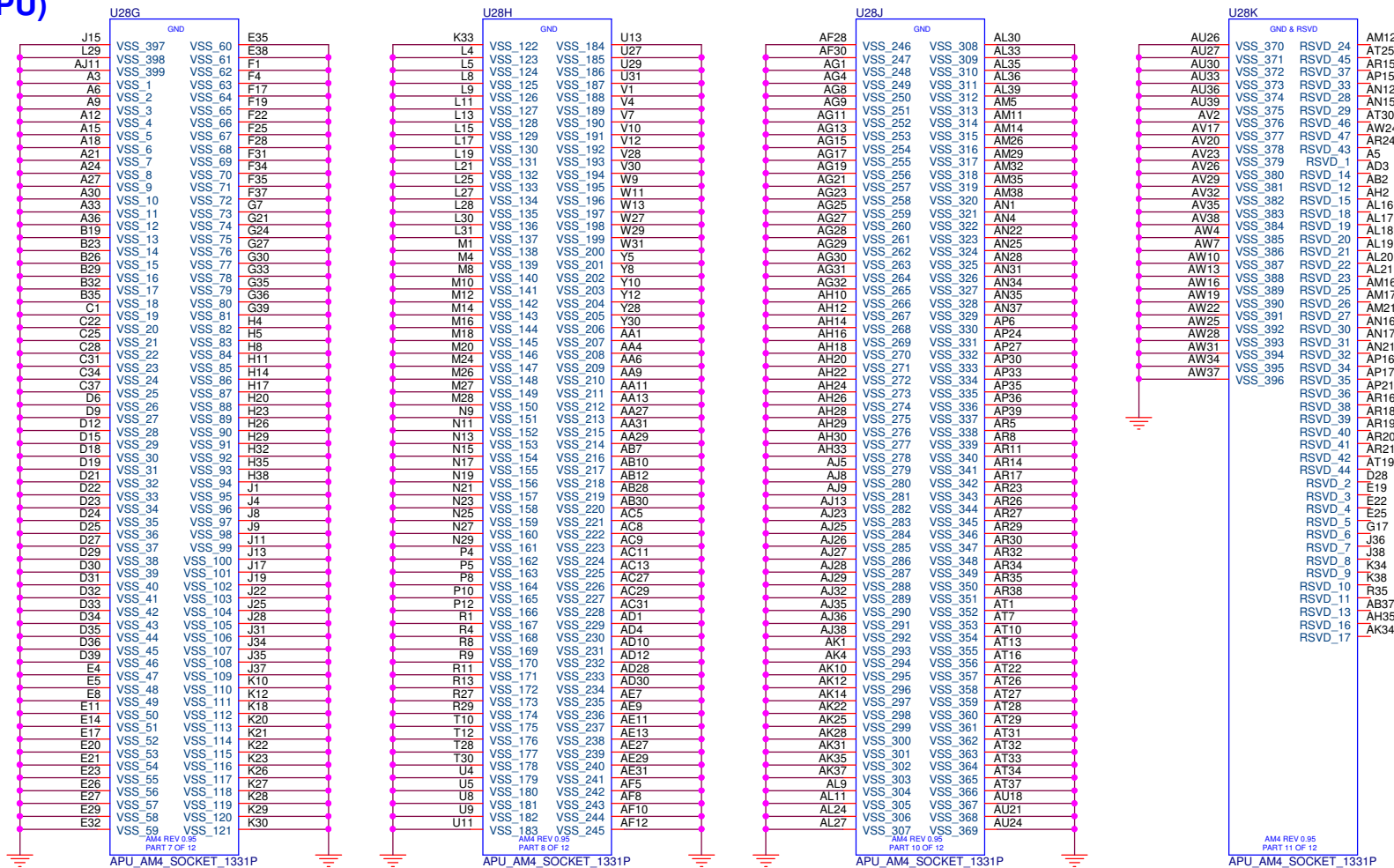




RTC(RTC)

(CPU)

08



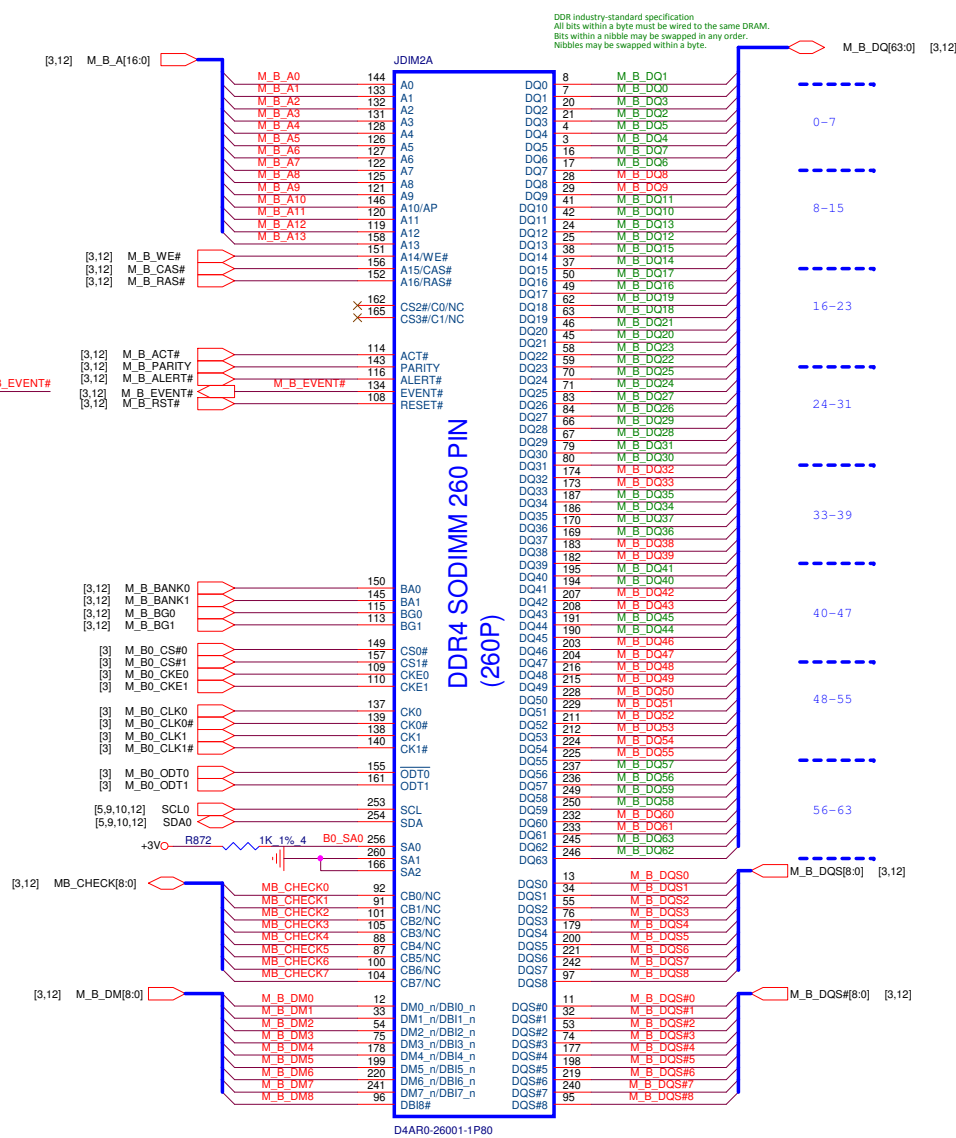


Address A0



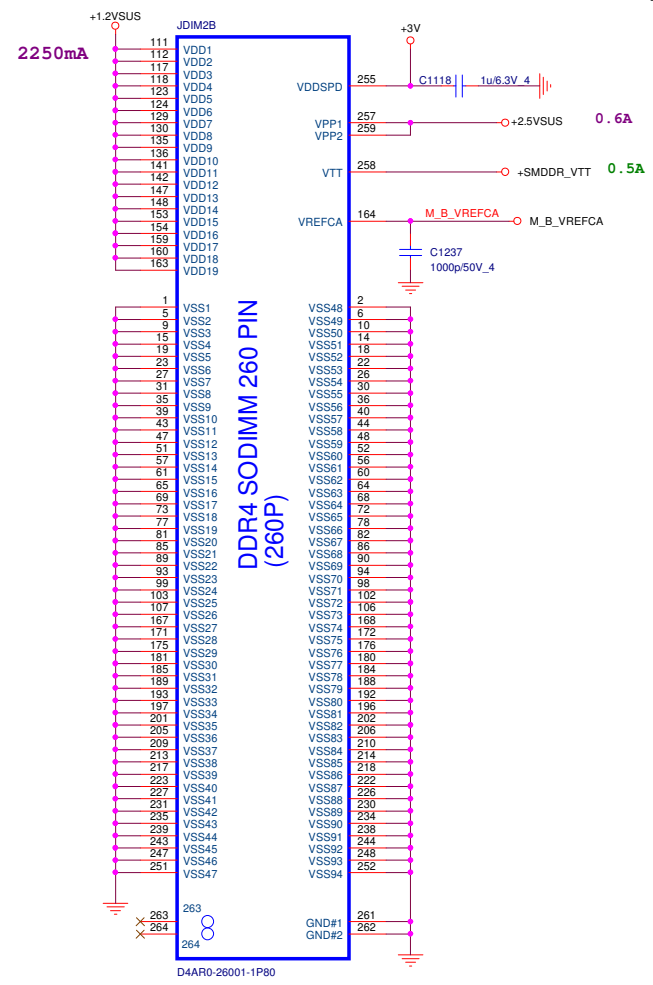
SODIMM (SDM)

Address A2



DDR4 SODIMM 260 PIN  
(260P)

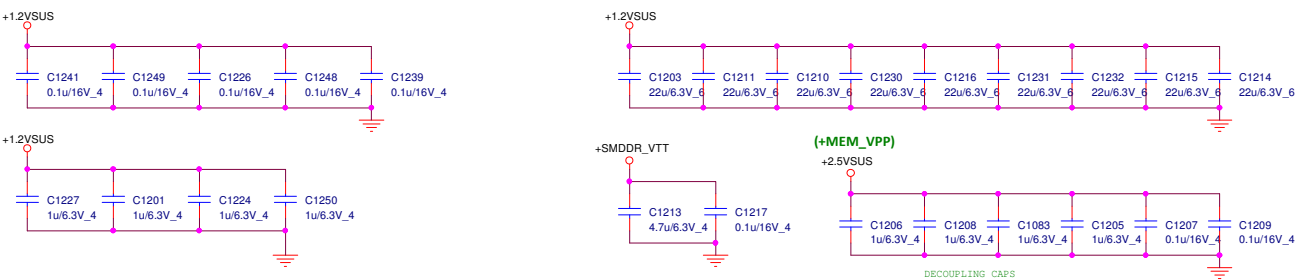
D4AR0-26001-1P80



DDR4 SODIMM 260 PIN  
(260P)

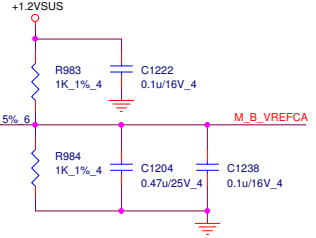
D4AR0-26001-1P80

Place these Caps near So-Dimm B0



From Power Chip (+0.6V)

+SMDDR\_VREF



Quanta Computer Inc.  
PROJECT : ZGX

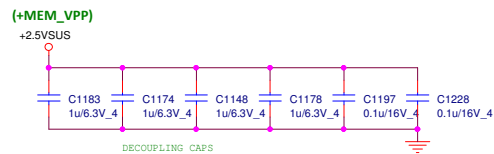
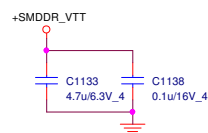
Size	Document Number	Rev
	DDR4 DIMM CHB0 (RVS-H4-T)	1A
Date:	Tuesday, June 26, 2018	Sheet 11 of 59

### Address A6

DDR industry-standard specification  
All bits within a byte must be wired to the same DRAM  
Bits within a nibble may be swapped in any order.  
Nibbles may be swapped within a byte.

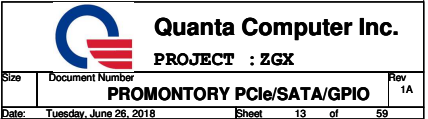


The image displays two circuit diagrams. The top diagram shows a +1.2V<sub>SUS</sub> supply connected to a series of five capacitors (C1251, C1240, C1252, C1223, C1235) connected in parallel to ground. Each capacitor is labeled with its value: 0.1u/16V\_4. The bottom diagram shows a similar setup with a +1.2V<sub>SUS</sub> supply connected to four capacitors (C1234, C1236, C1225, C1212) in parallel to ground. These capacitors are labeled with values: 1u/6.3V\_4, 1u/6.3V\_4, 1u/6.3V\_4, and 1u/6.3V\_4 respectively.

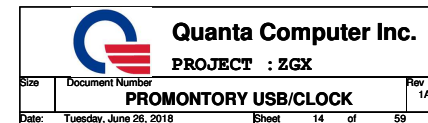


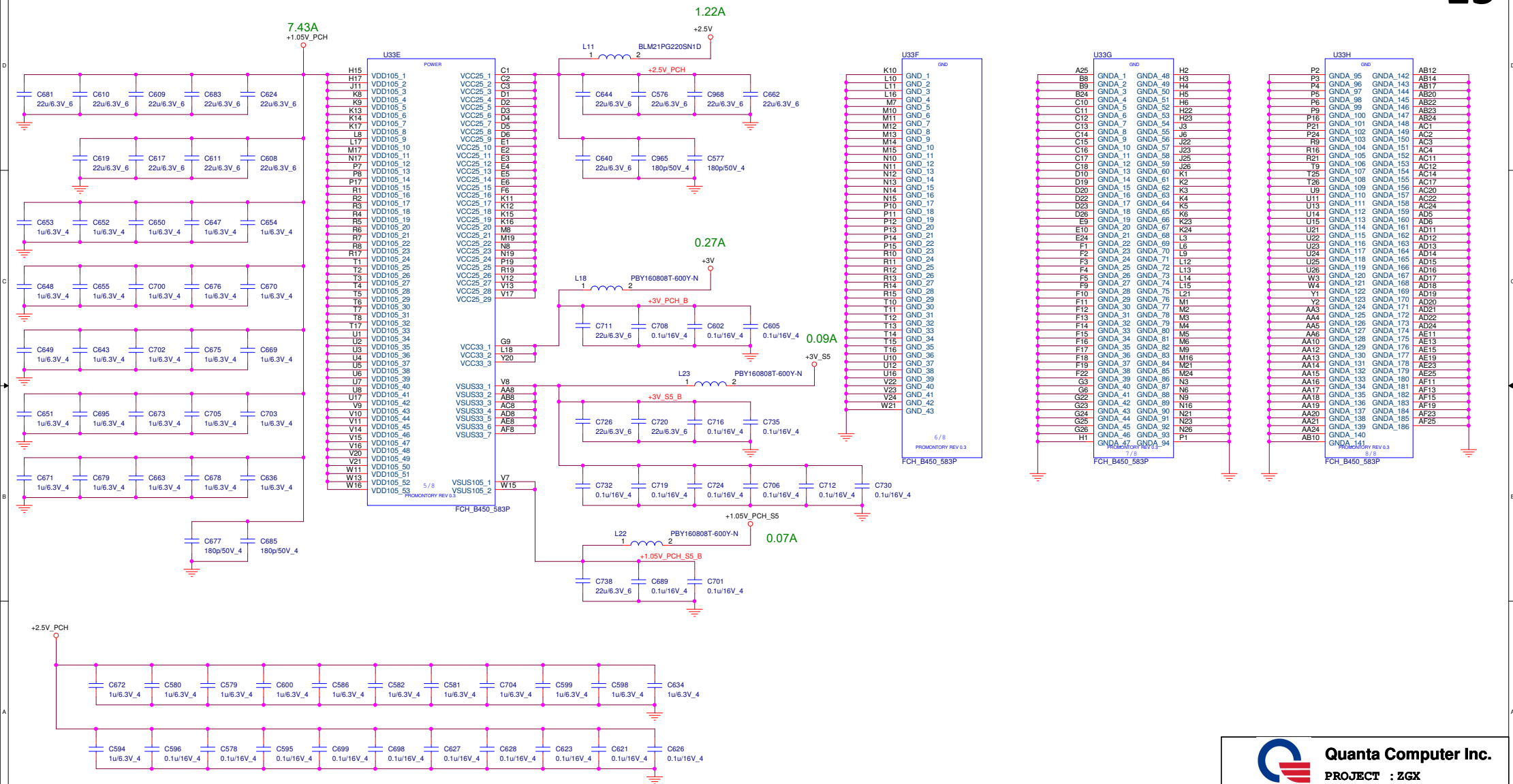
**DDR4 DIMM CHB1 (RVS-H9-B)**

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## GPU (VGA)



GFX (RR)

SR)

GFX (RR)

gnd voids underneath

### Power up sequence and entry mode(PX\_EN=1)

16



CTF:  
High (+3.3v) : critical temperature fault occurs  
Low: dGPU operator normally as default



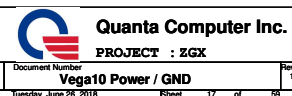
**Quanta Computer Inc.**

**PROJECT : ZGX**

### Vega10 PCIe Interface

Size	Document Number	Rev
	<b>Vega10 PCIe Interface</b>	1A
Date:	Tuesday, June 26, 2018	Sheet 16 of 59

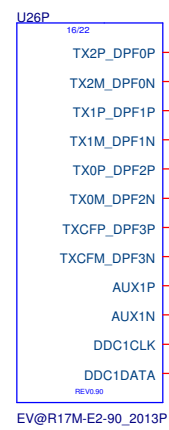
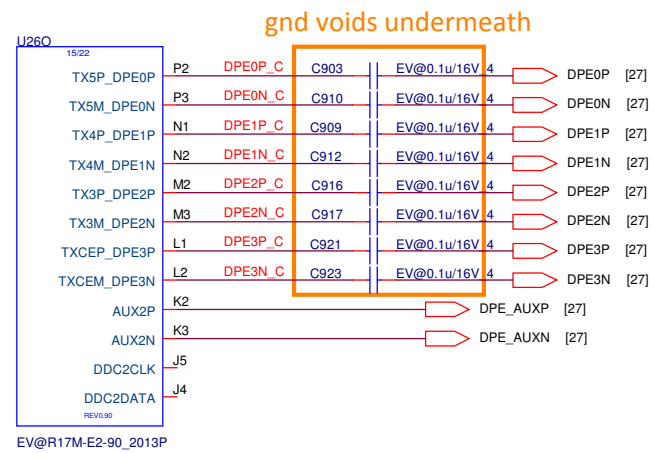
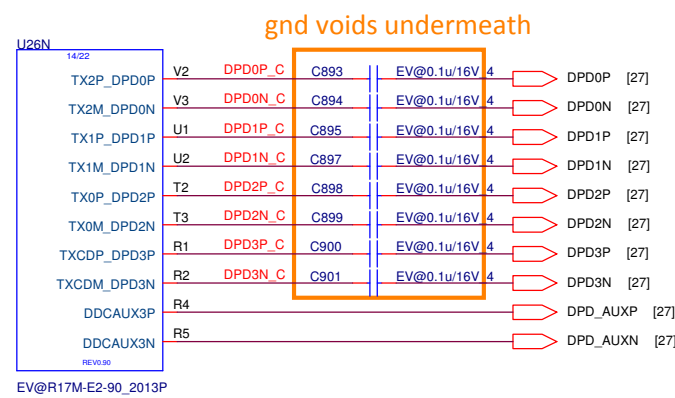
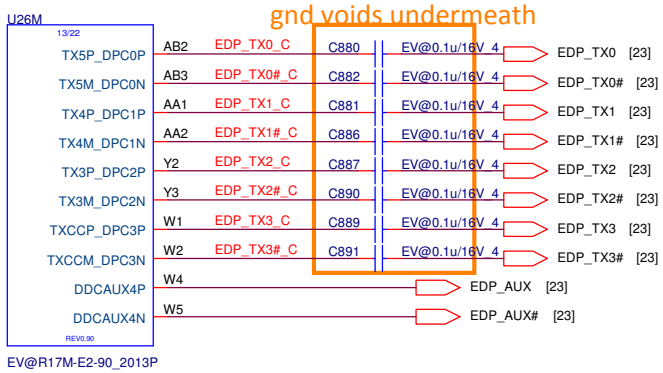
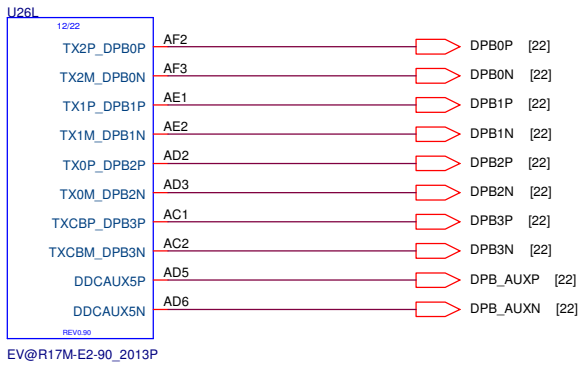
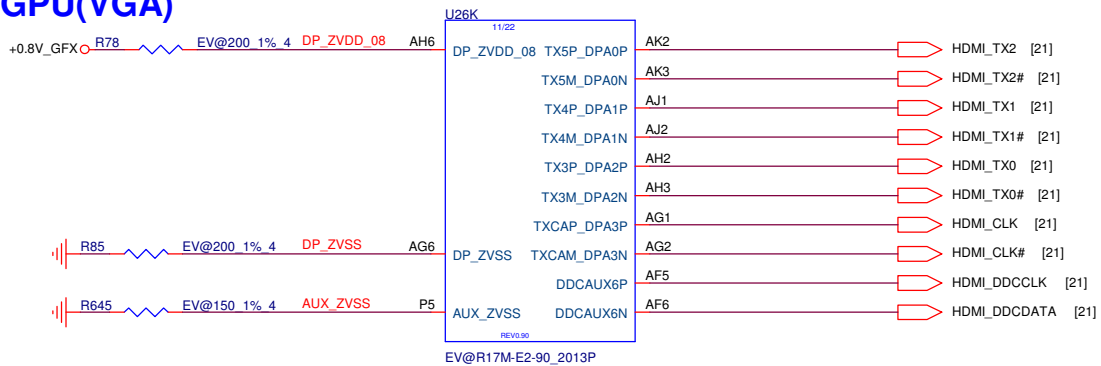
Date: Tuesday, June 26, 2018 Sheet 16 of 59





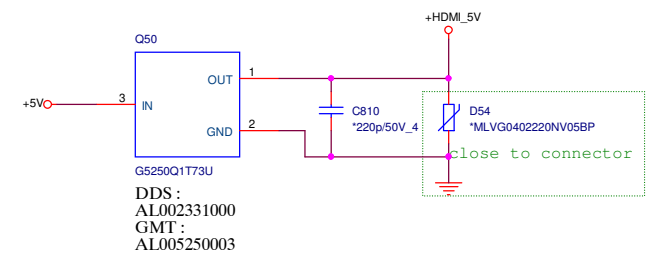
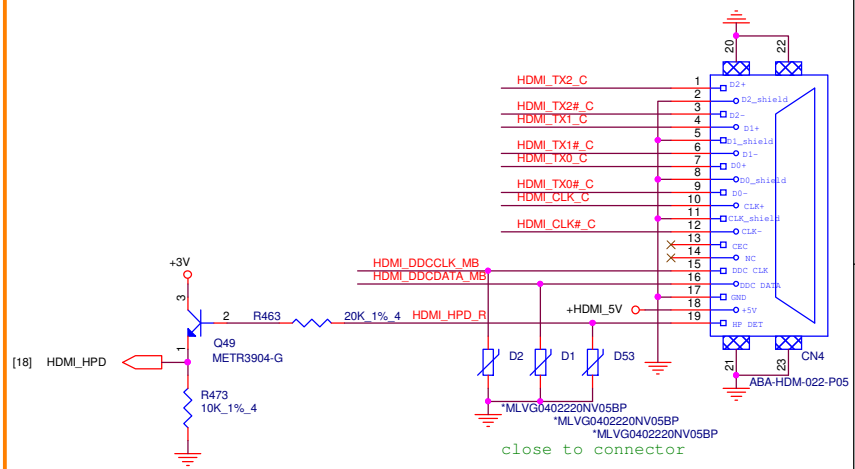
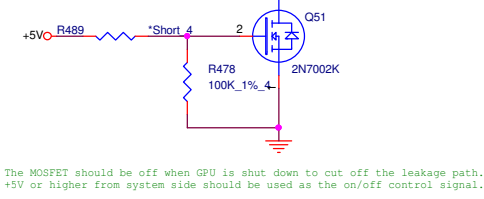
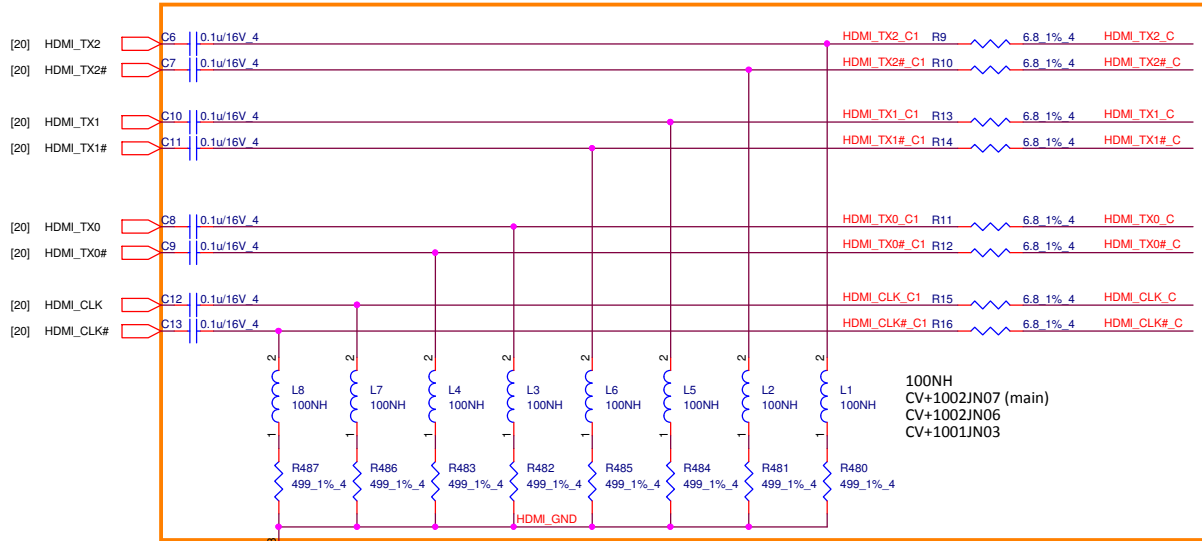




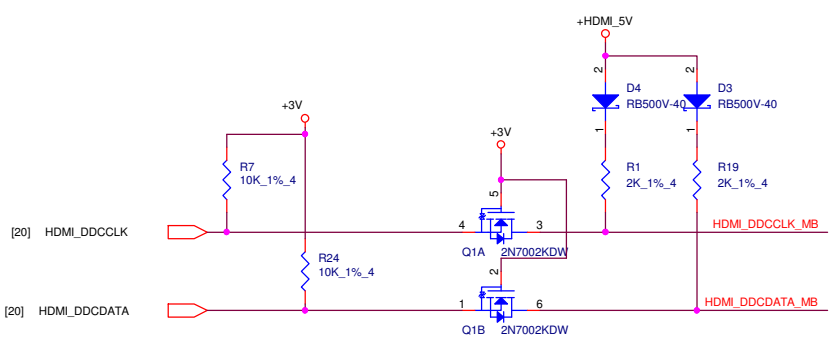


HDMI(HDM)

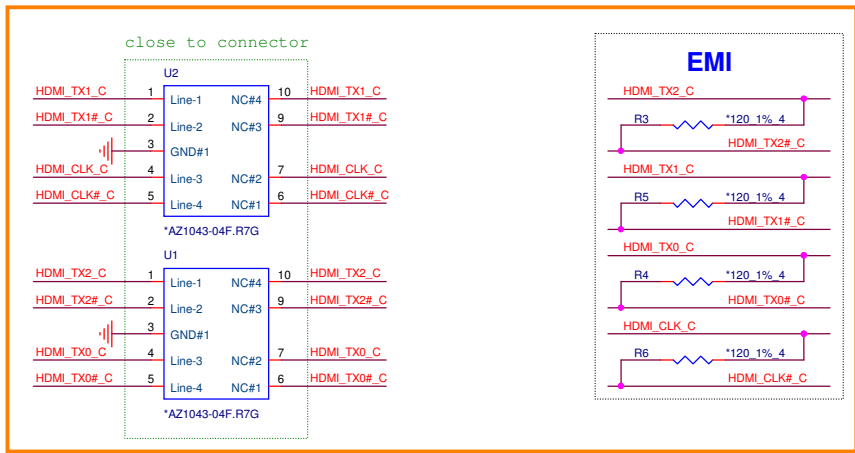
gnd voids underneath



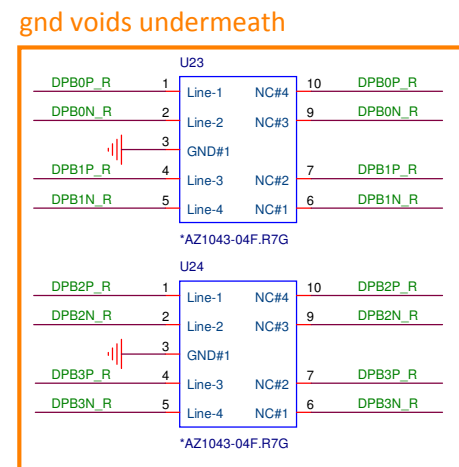
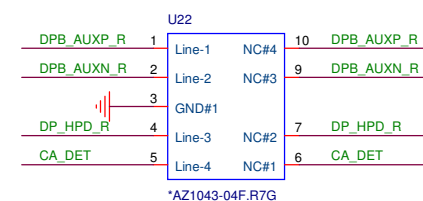
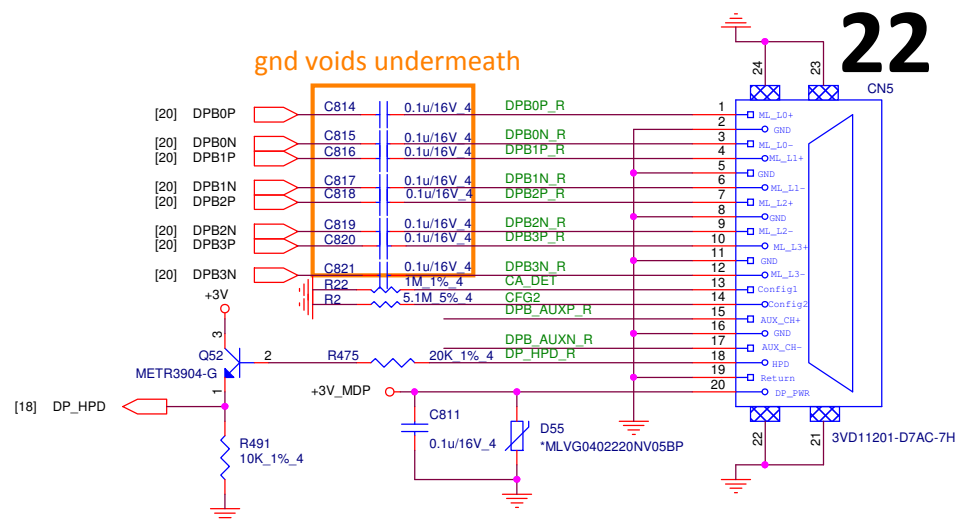
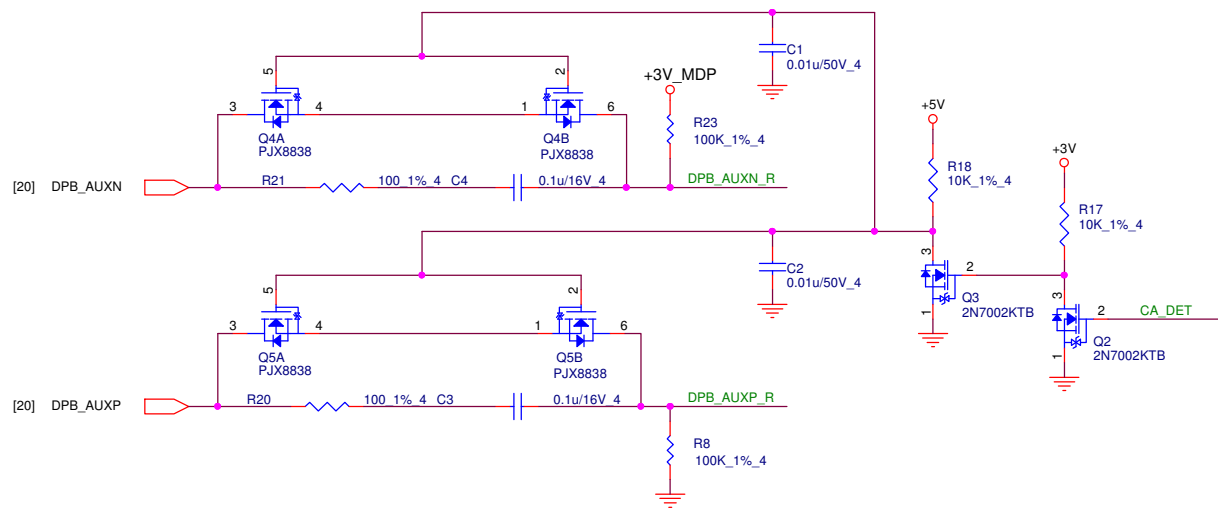
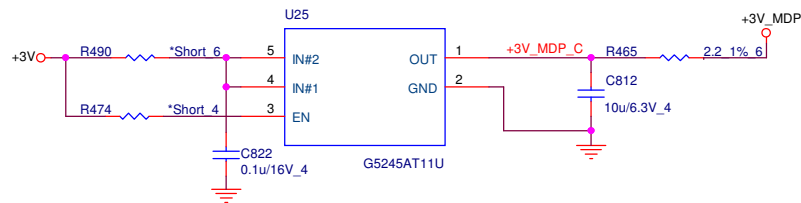
HDMI DDC (HDM)



gnd voids underneath



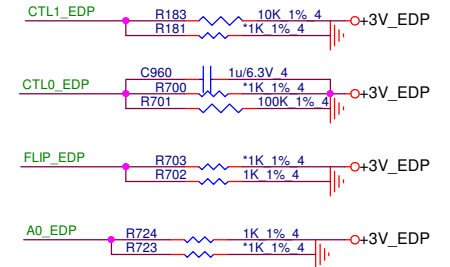
# Display Port (DPP)



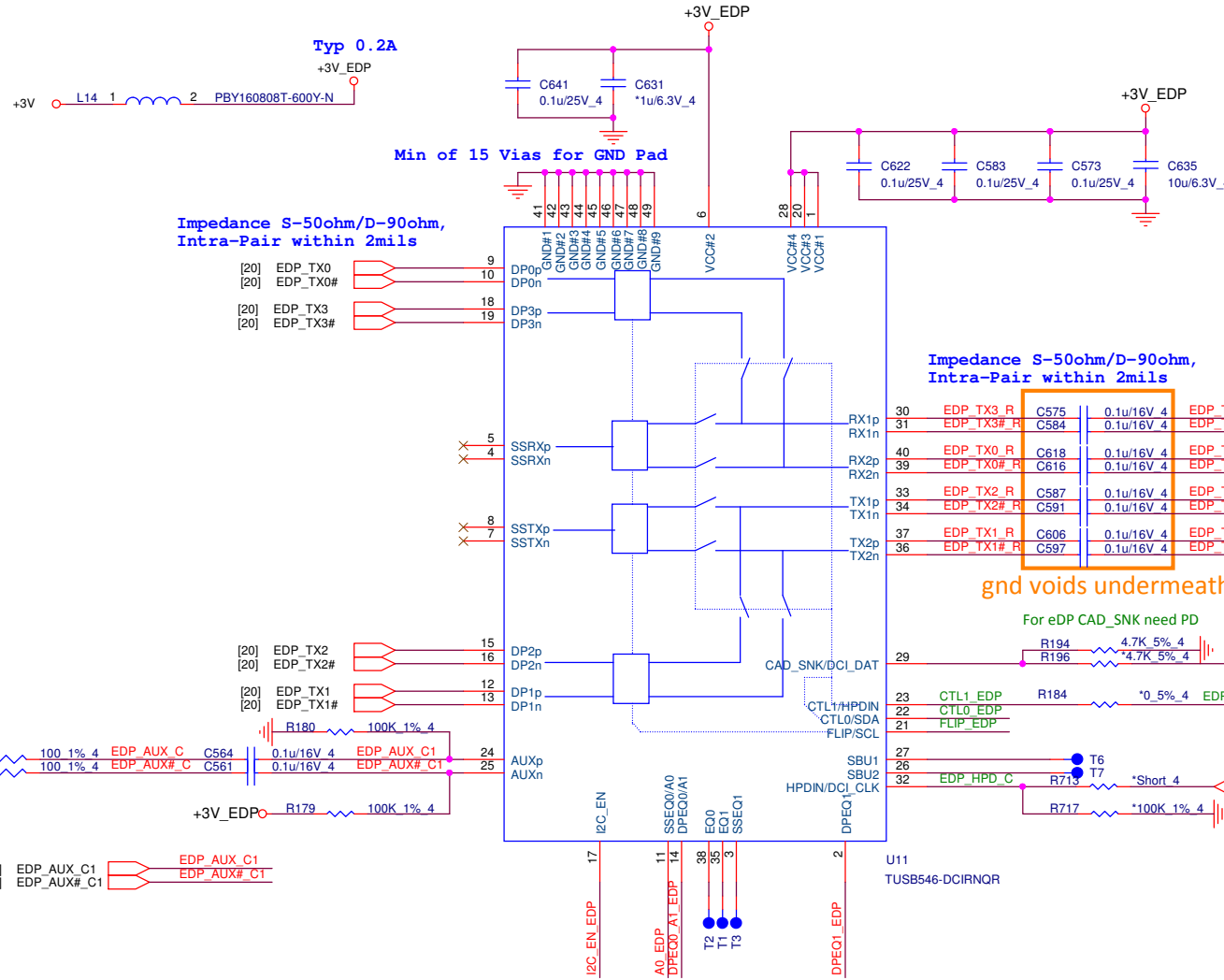
# eDP Redriver (LDS)

23

Four Lane DP-No Filp  
CTL1=H, CTL0=L, FILP=L



SSEQ0, SSEQ1 : USB receiver equalizer gain for upstream facing SSTXP/N  
F,F (Default)  
When I2C\_EN is not '0' SSEQ0 sets I2C address



gnd voids underneath

For eDP CAD\_SNK need PD

PN OK

I2C Programming or pin strap programming select.  
I2C is only disable when this pin is '0'  
0 : Pin Strap(I2C disable) (Default)  
R : TI test mode(I2C enable at 3.3V)  
F : I2C enabled at 1.8V  
1 : I2C enabled at 3.3V

DPEQ0, DPEQ1 : DP Receiver equalization gain  
F,F (Default)  
When I2C\_EN is not '0' DPEQ0 sets I2C address



Quanta Computer Inc.

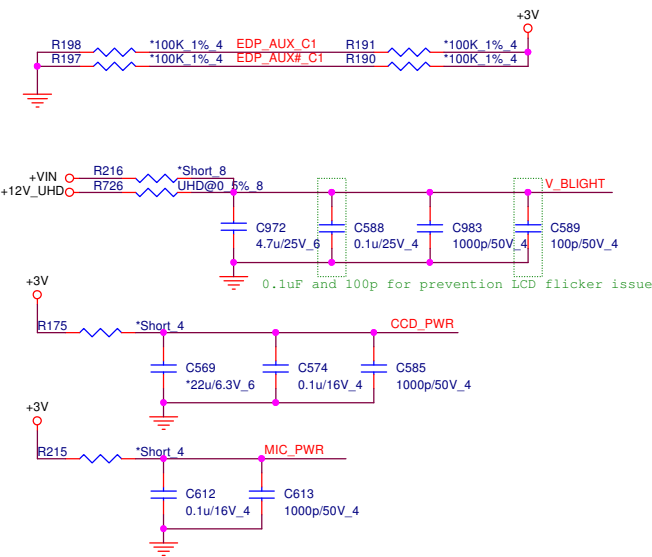
PROJECT : ZGX

Size	Document Number	Rev
	eDP re-Driver	1A

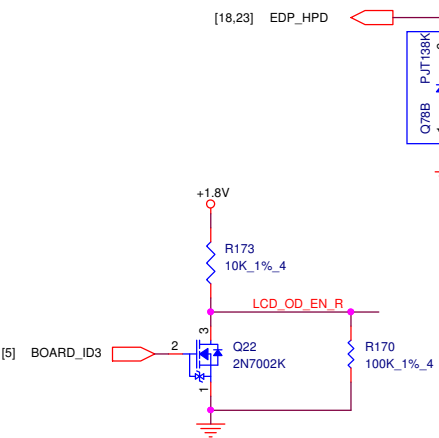
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LCD (LDS)



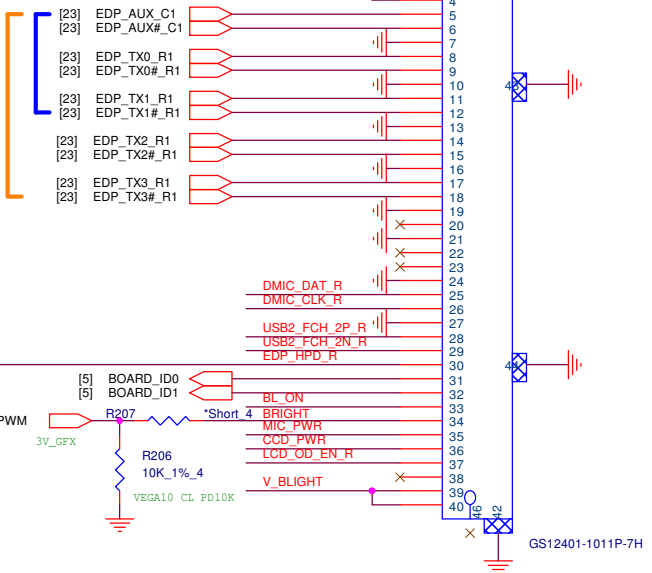
Panel ID 1	Panel ID 0	OD_EN	PWM pin	NVSR pin (FRAME_LOCK#)	Support panel	Remark
0	0	NC			Reserve	Panel ID 0,1 connect to GND in cable
0	1	NC	NC	Y	NVSR	Panel ID 1 connect to GND in cable
1	0	Y	Y	NC	DD	Panel ID 0 connect to GND in cable
1	1	NC	Y	NC	Normal, Freesync	Panel ID 0,1 NC in cable



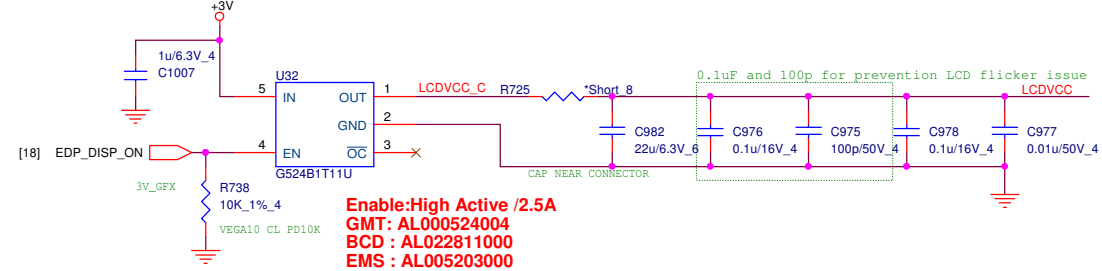
Function	Enable	Disable
LCD_OD_EN_R	Hi or Open	Default

eDP FHD

eDP UHD

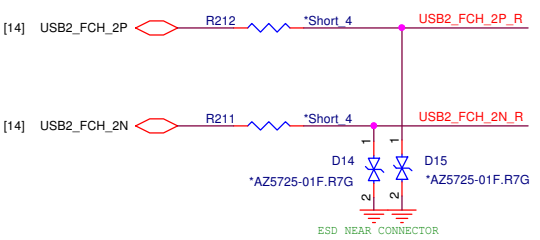


LCD Power (LDS)

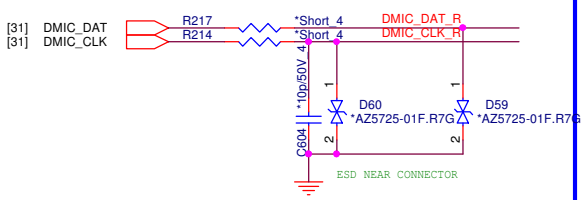


Enable:High Active /2.5A  
GMT : AL000524004  
BCD : AL022811000  
EMS : AL005203000

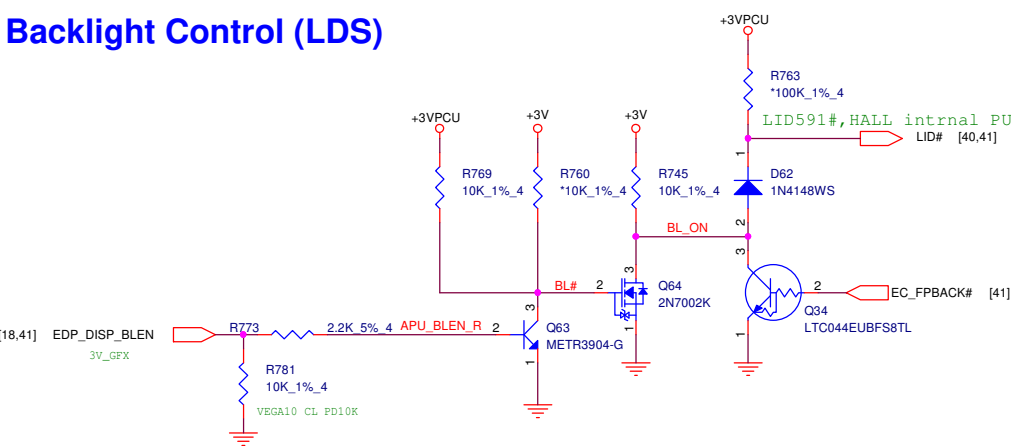
Front Camera (FCM)




Microphone (MIC)



Backlight Control (LDS)

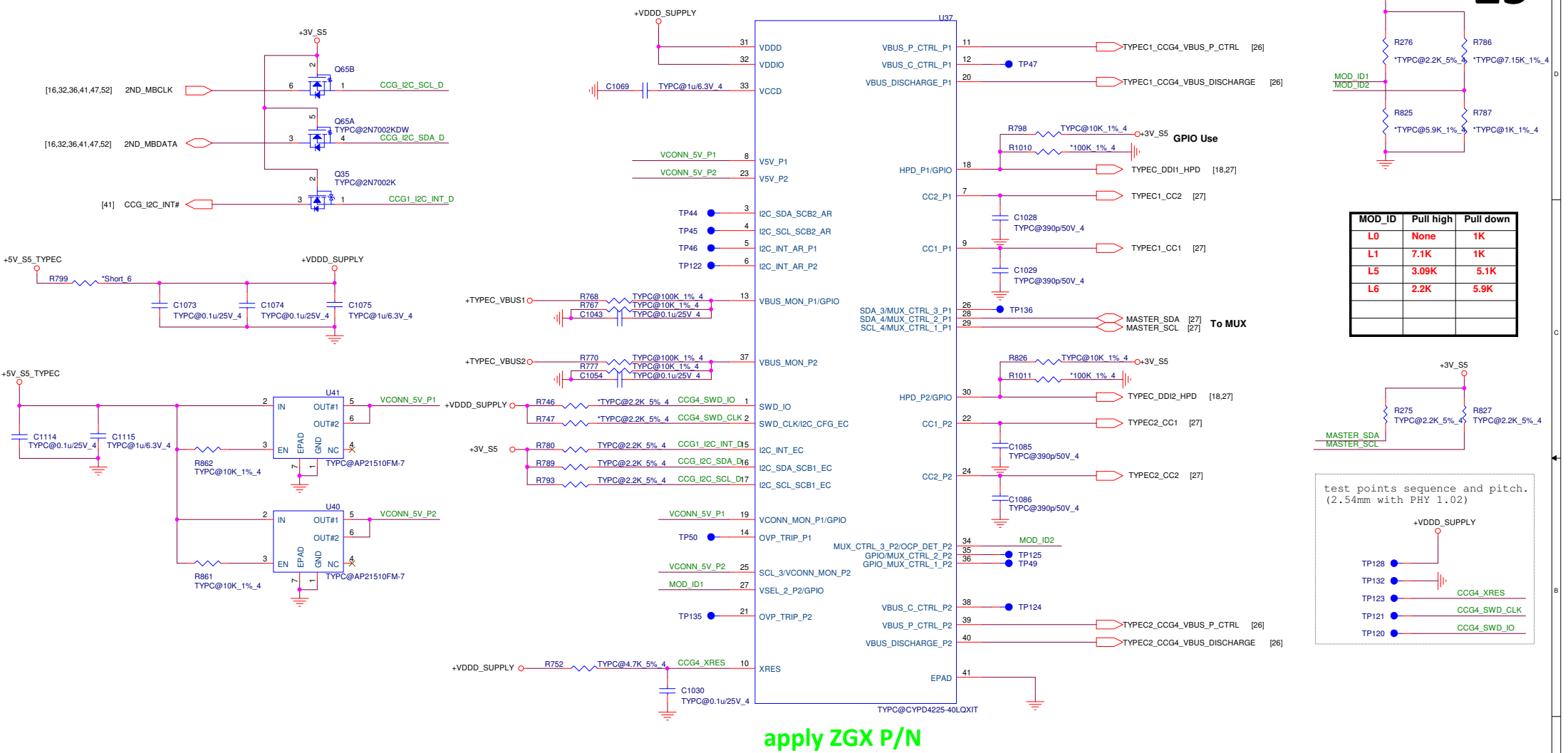




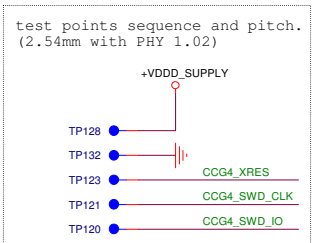
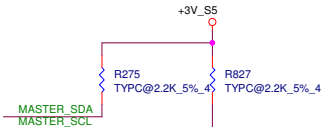
**Quanta Computer Inc.**  
**PROJECT : ZGX**

Size	Document Number	Rev
	<b>eDP Panel/CCD/Hall Sensor</b>	<b>1A</b>
Date:	Tuesday, June 26, 2018	Sheet 24 of 59

# Cypress CCG4 (UTC)



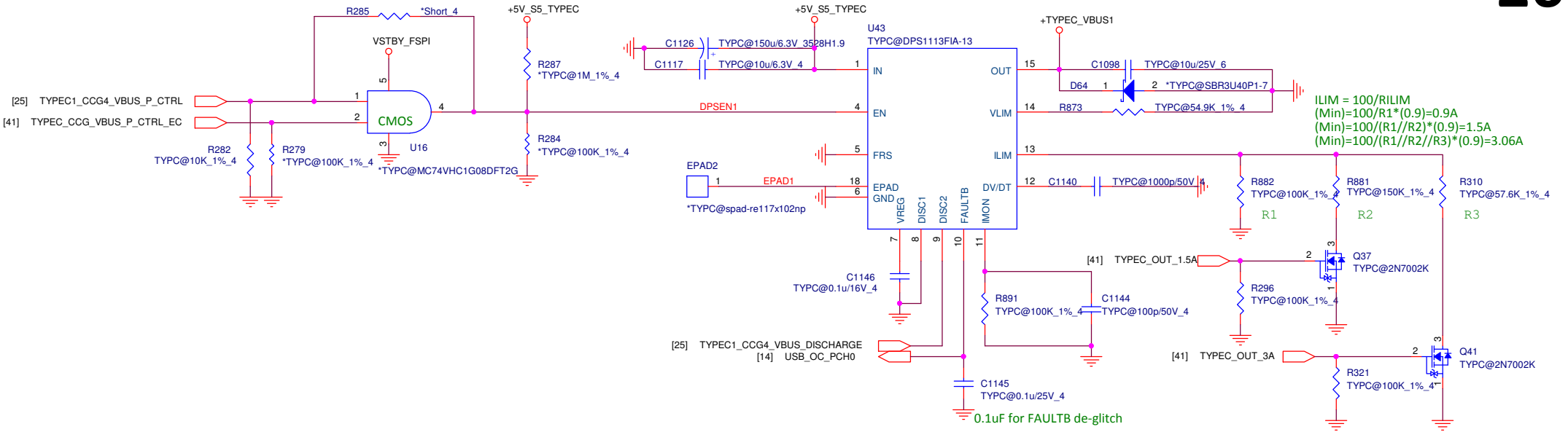
MOD_ID	Pull high	Pull down
L0	None	1K
L1	7.1K	1K
L5	3.09K	5.1K
L6	2.2K	5.9K



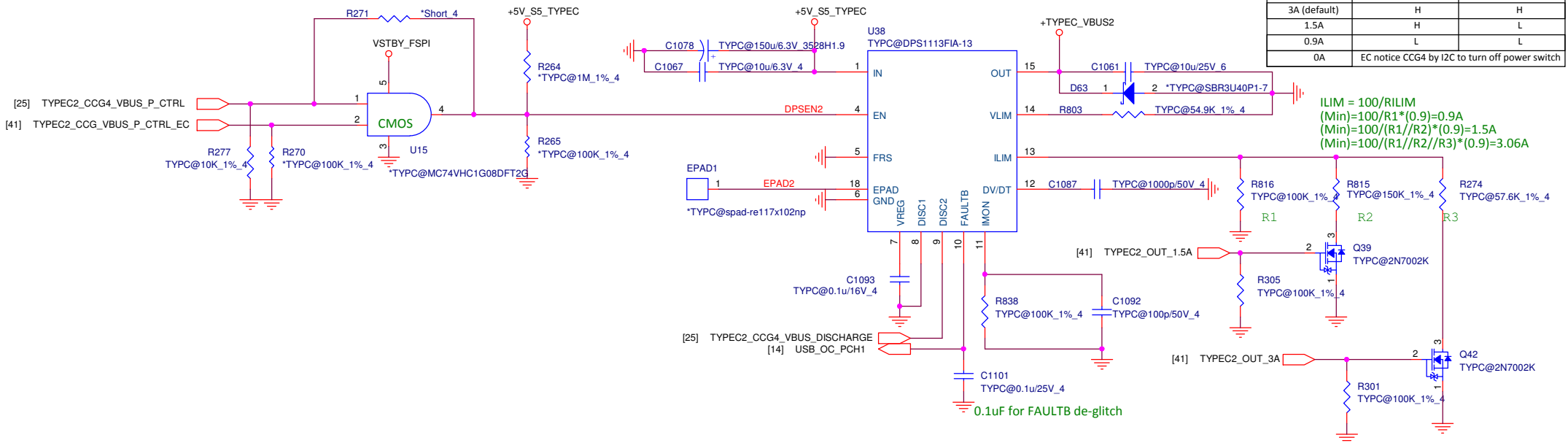
apply ZGX P/N

# Type C Power switch (UTC)

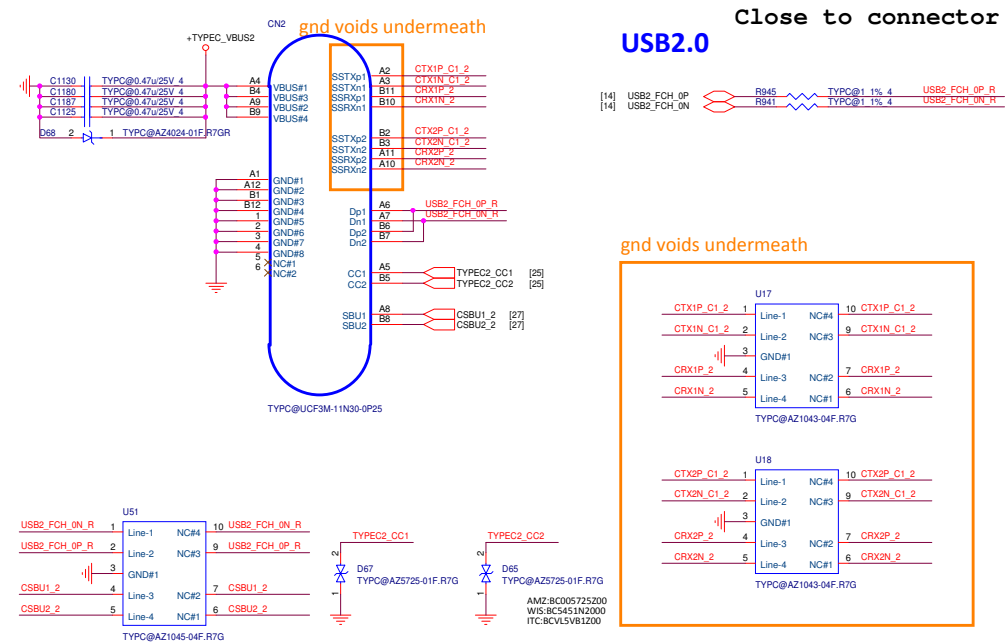
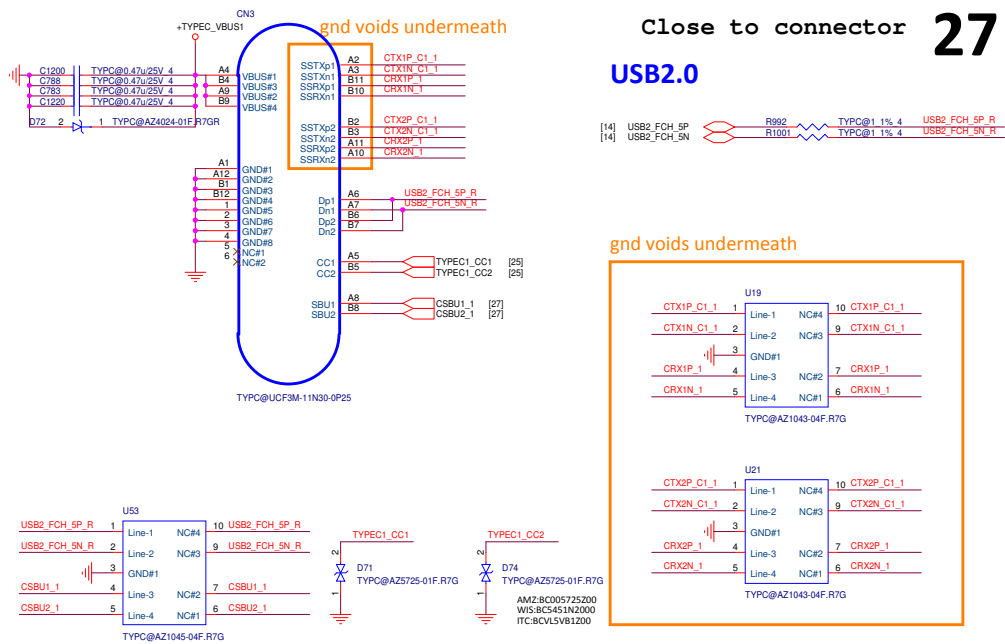
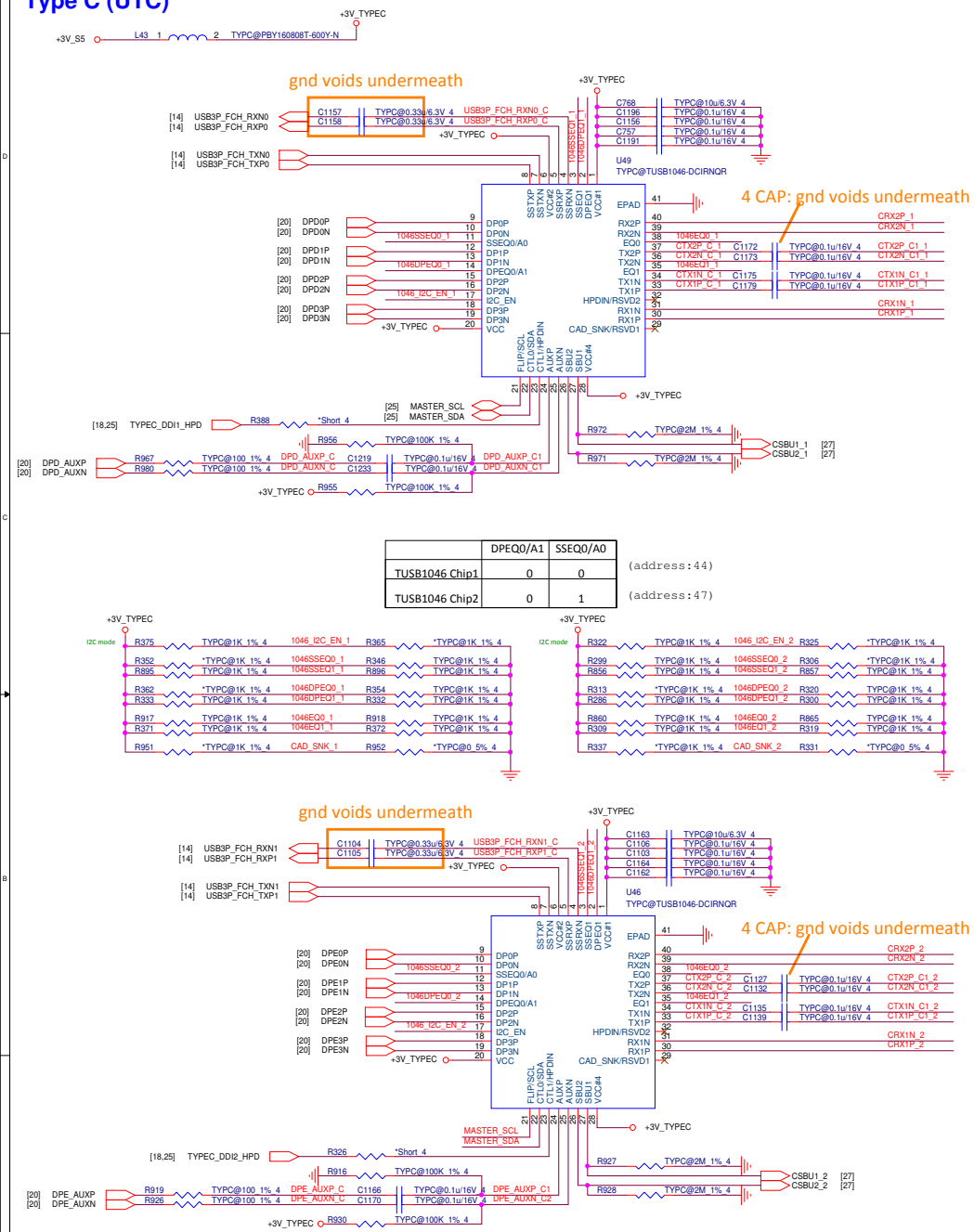
26

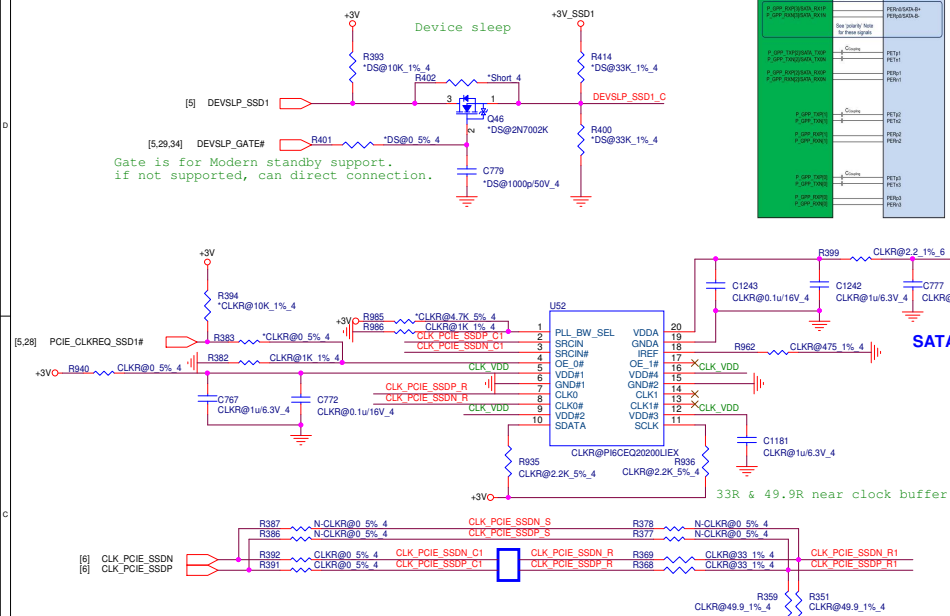


USB Type-C Port	TYPEC_OUT_1.5A	TYPEC_OUT_3A
3A (default)	H	H
1.5A	H	L
0.9A	L	L
0A	EC notice CCG4 by I2C to turn off power switch	

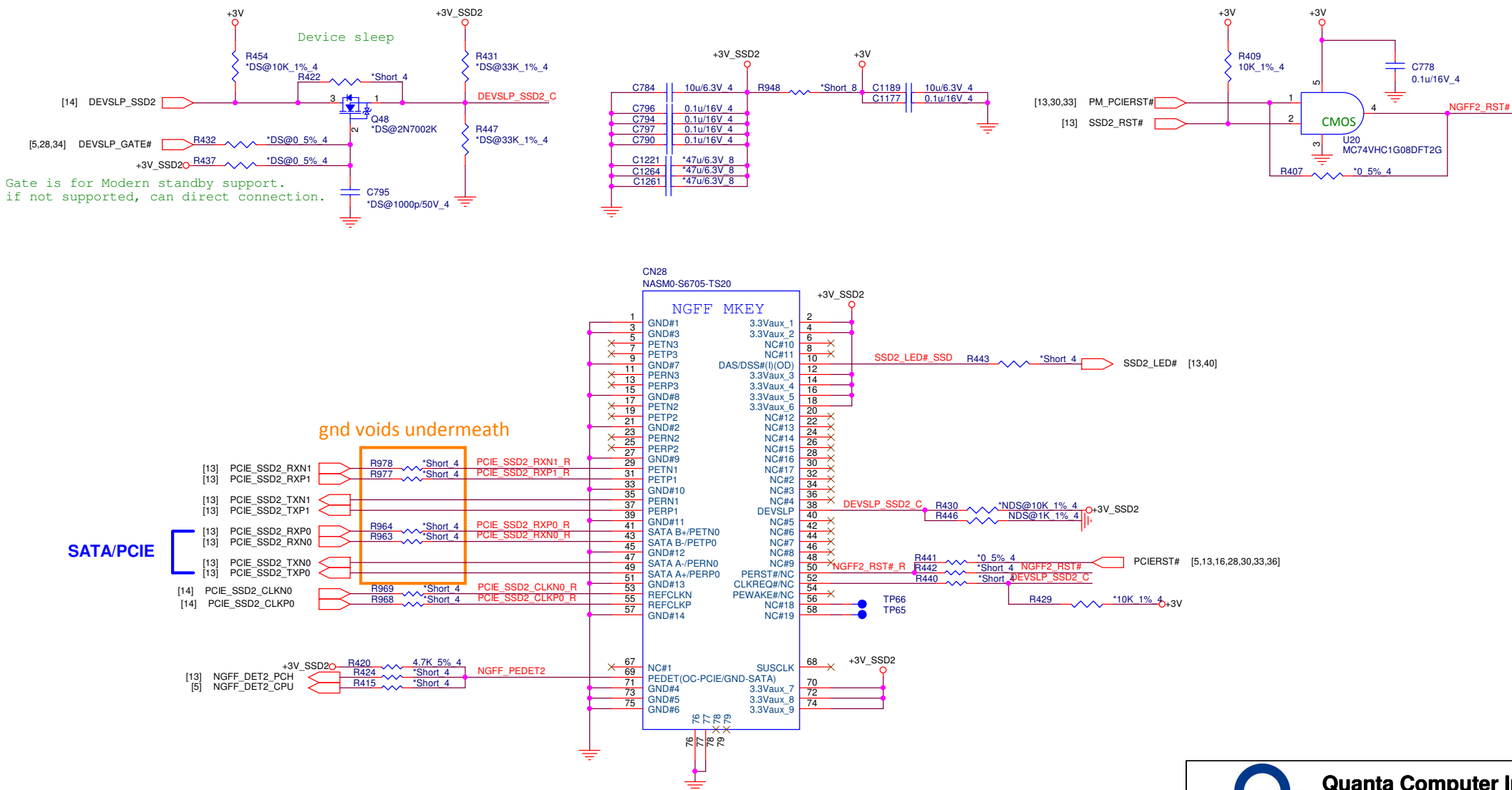


## Type C (UTC)



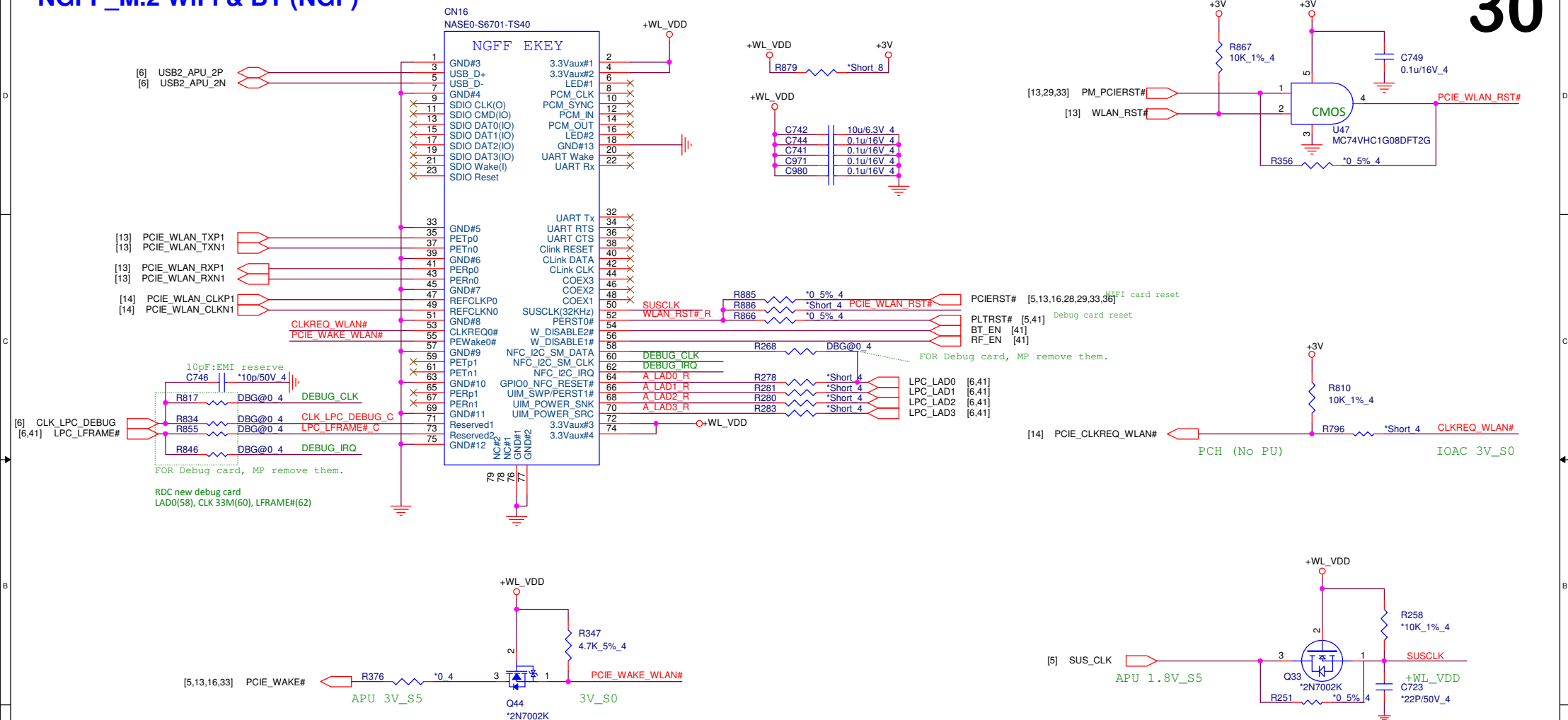




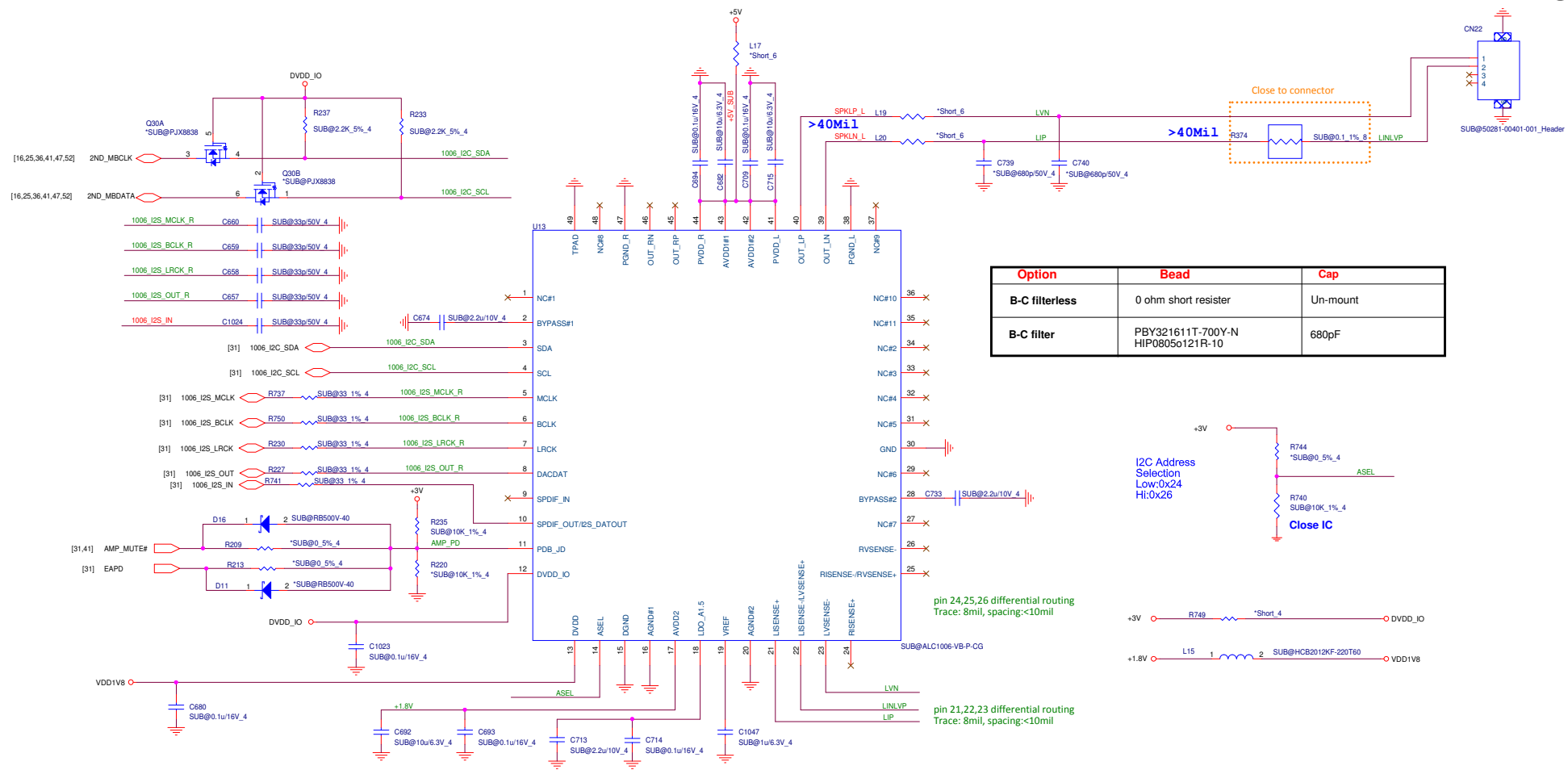


# NGFF\_M.2 WiFi & BT (NGF)

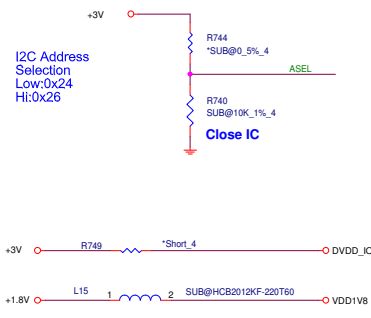
30







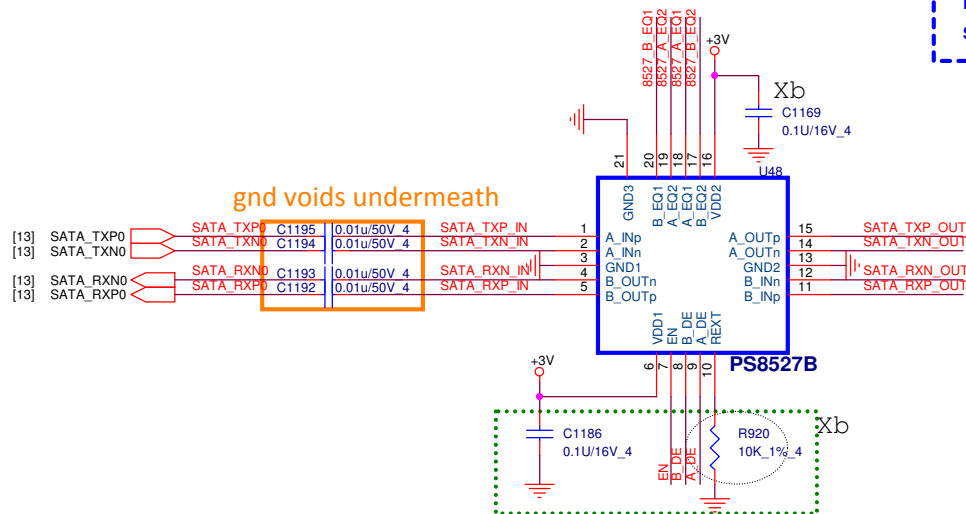
Option	Bead	Cap
B-C filterless	0 ohm short resistor	Un-mount
B-C filter	PBY321611T-700Y-N HIP0805o121R-10	680pF



FP/PN OK



# HDD Re-driever(HDD)



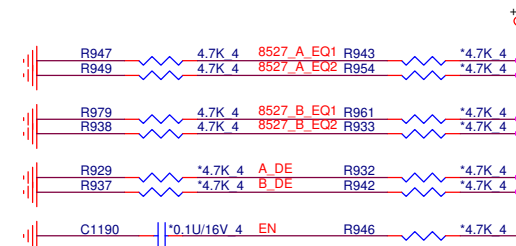
SATA re-driver IC  
stuff Rb,Cb,Xb , unstuff Ra,Ca

Normal  
stuff Ra,Ca , unstuff Rb,Cb

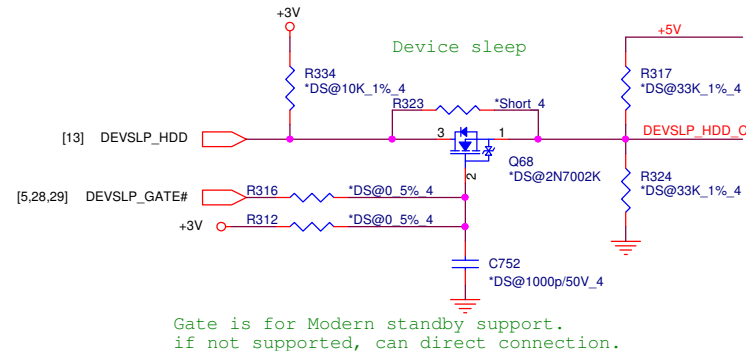
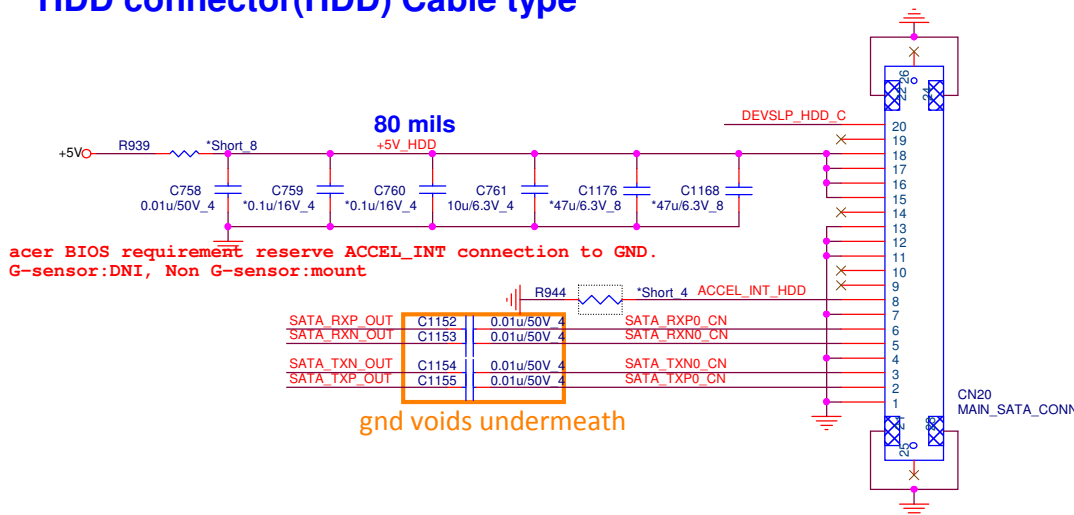
Equalization level setting for Channel x(x=A/B),internally tied to VDD/2 (default:12.2dB)  
[x\_EQ2, x\_EQ1] ==  
L/L: for channel loss up to 7.4dB  
L/H: for channel loss up to 14.4dB  
H/L: for channel loss up to 11.2dB  
H/H: for channel loss up to 5dB

De-emphasis level setting for Channel x(x=A/B), internally tied to VDD/2(Default=-3.5dB)  
[x\_DE] ==  
L: 0 dB  
H: -6dB

8/11 FAE suggest A\_EQ1,A\_EQ2,B\_EQ1,B\_EQ2 mount for LL EQ 7.4dB



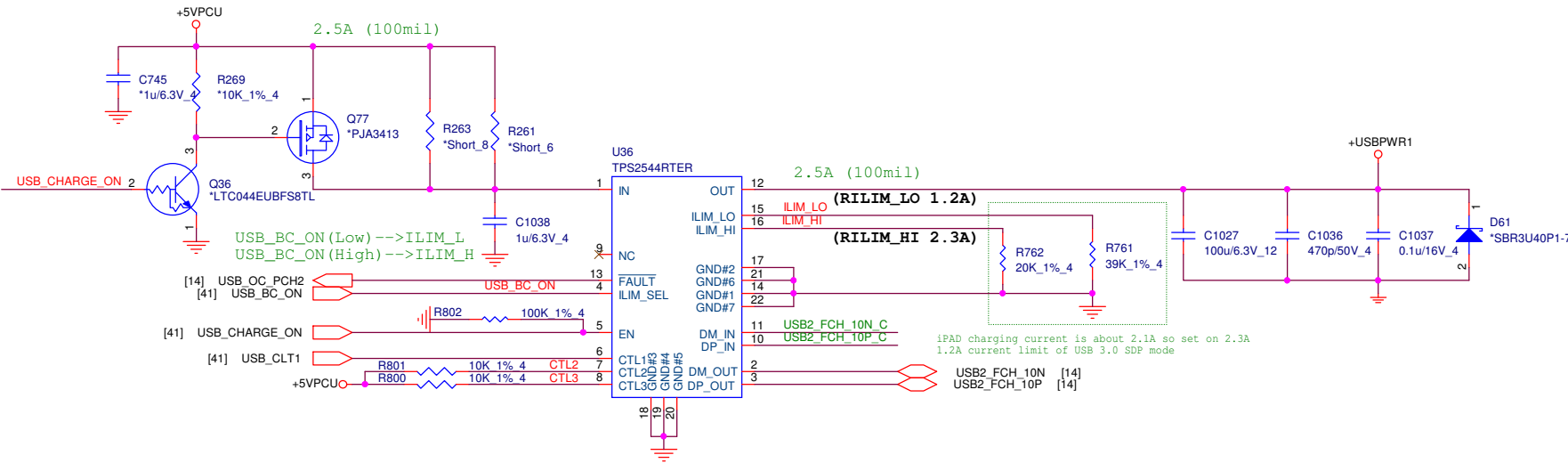
## HDD connector(HDD) Cable type



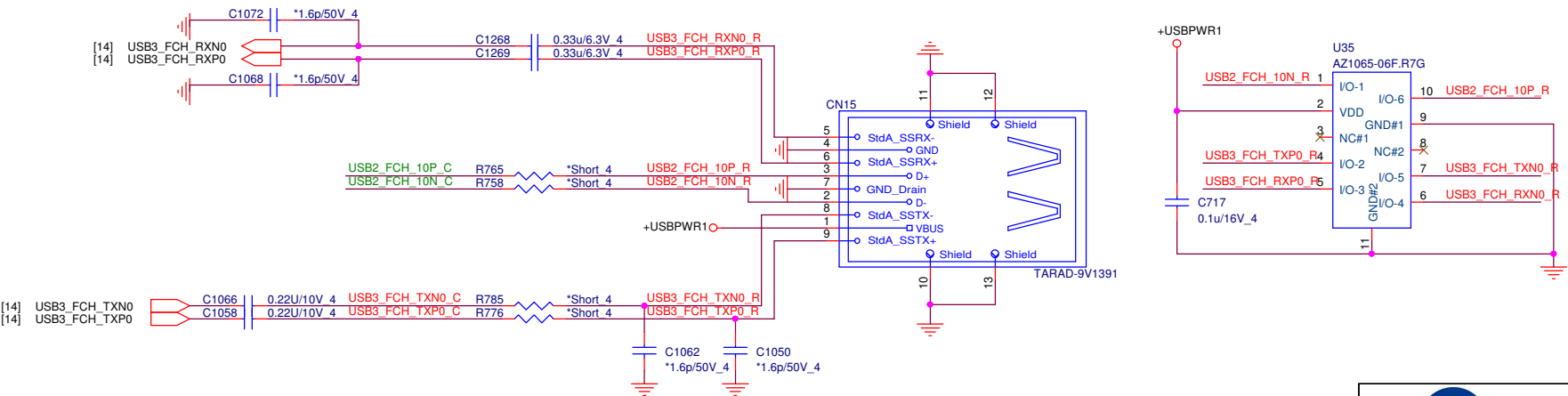
Quanta Computer Inc.  
PROJECT : ZGX

Size	Document Number	Rev
	HDD/Re-Driver	1A
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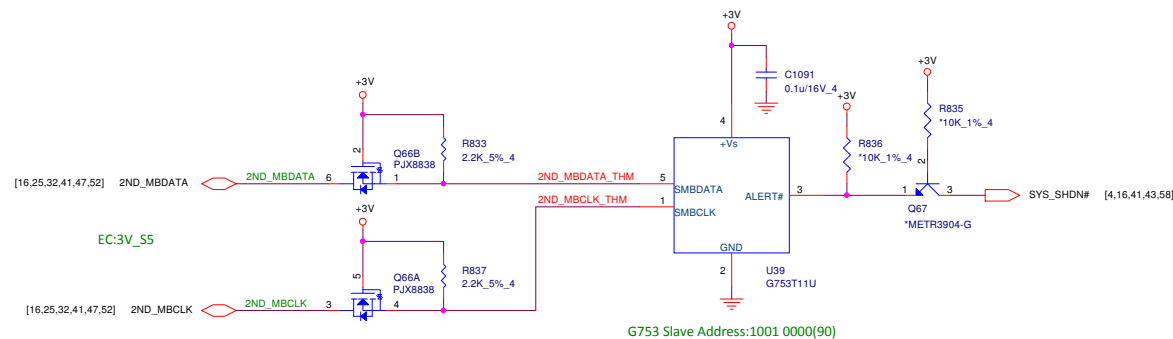
USB 3.0 (UB3) FROM PCH



## 12V-PWM



36

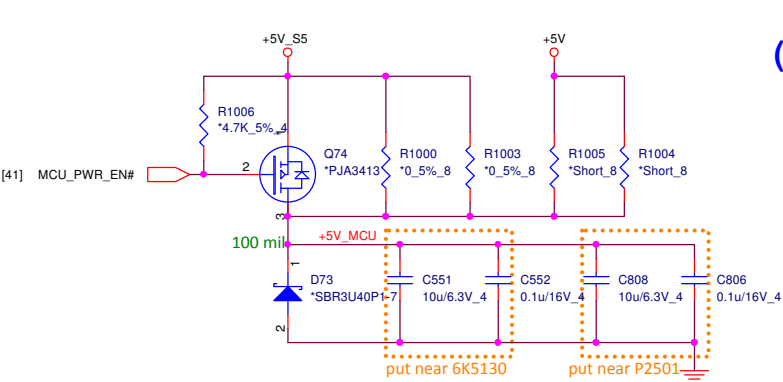


**PROJECT : ZGX**

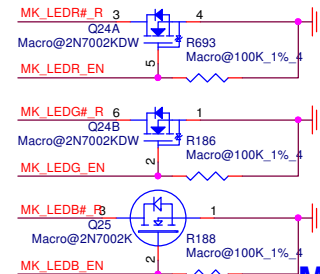
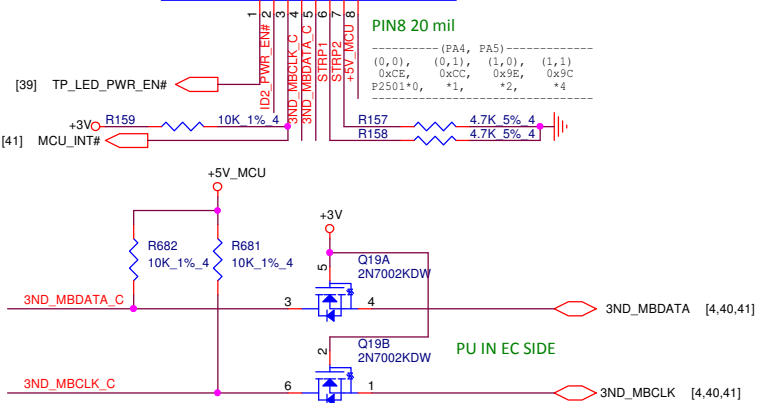
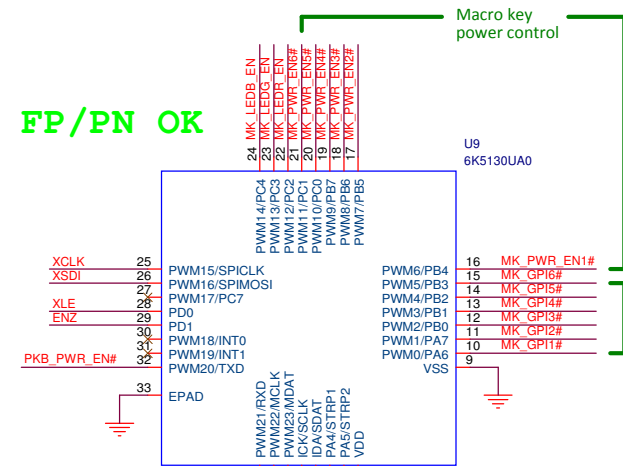
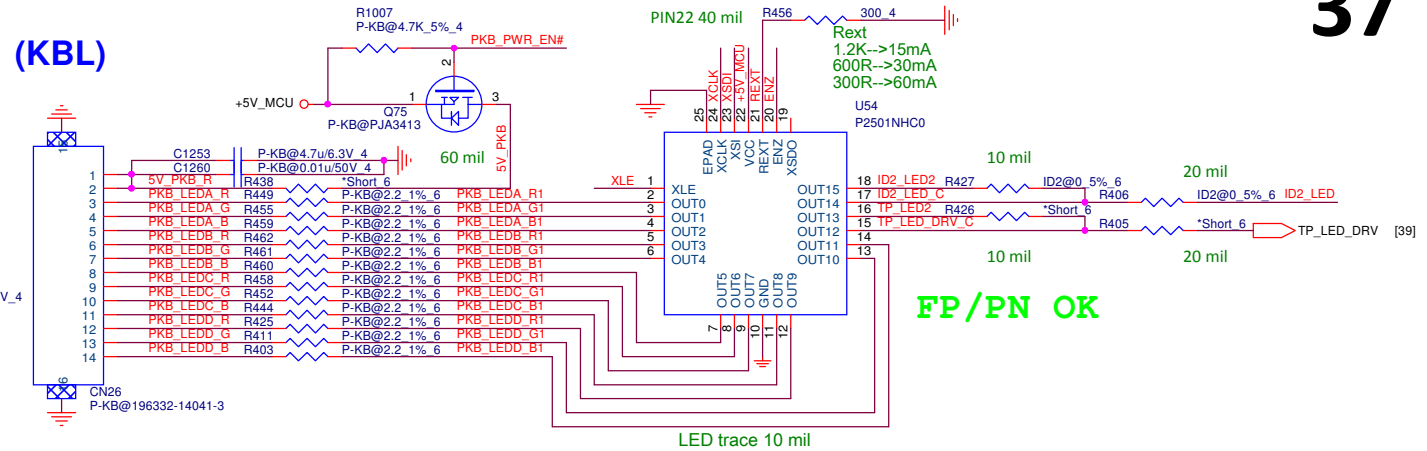
Size	Document Number	Rev
	<b>FAN/Thermal/Xbox/Tobii</b>	1A
Date:	Tuesday, June 26, 2018	Sheet 36 of 59

# UIF Controller (UIF)

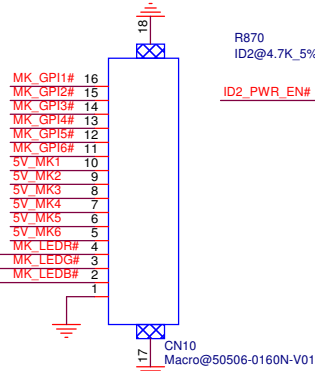
37



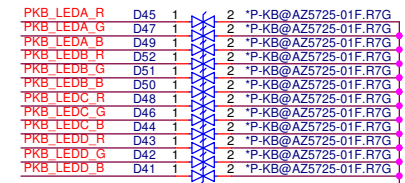
## (KBL)



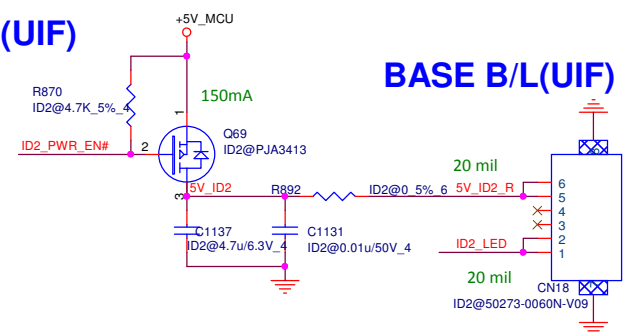
## Macro Key (UIF)



FP/PN OK



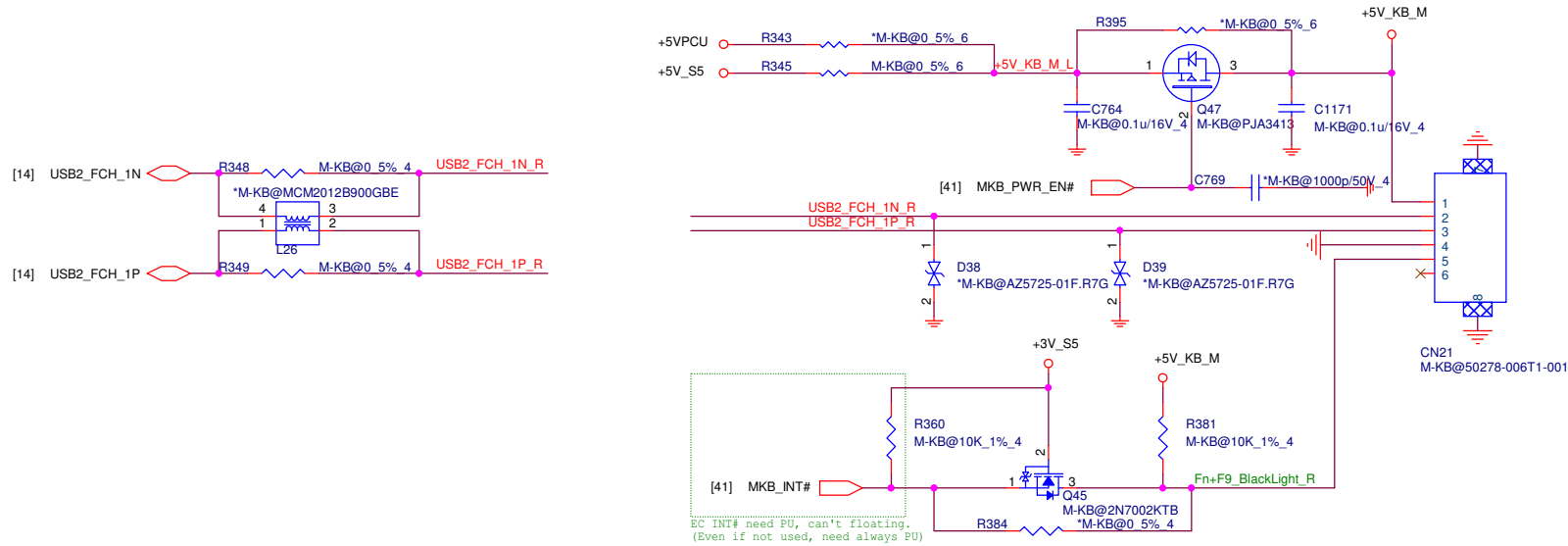
## BASE B/L(UIF)



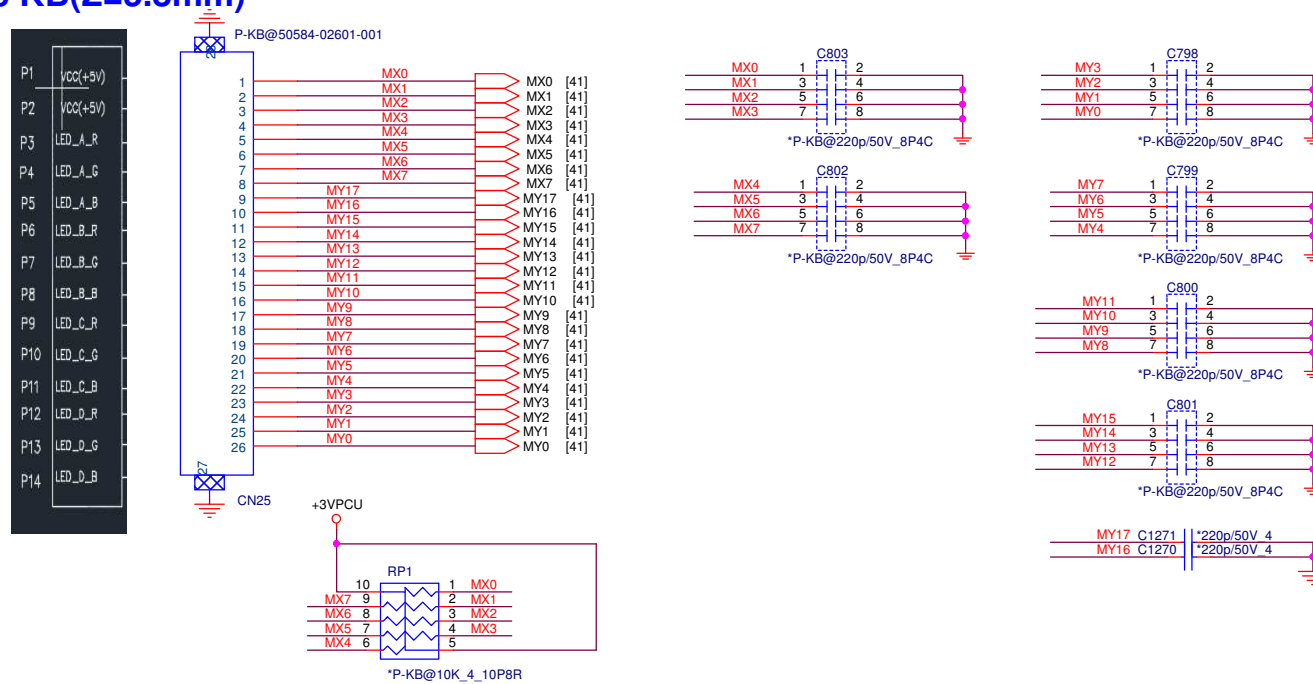
**Quanta Computer Inc.**  
PROJECT : ZGX

Size	Document Number	Rev
	MCU/Macro Key/KBL/ID2/BAS	1A
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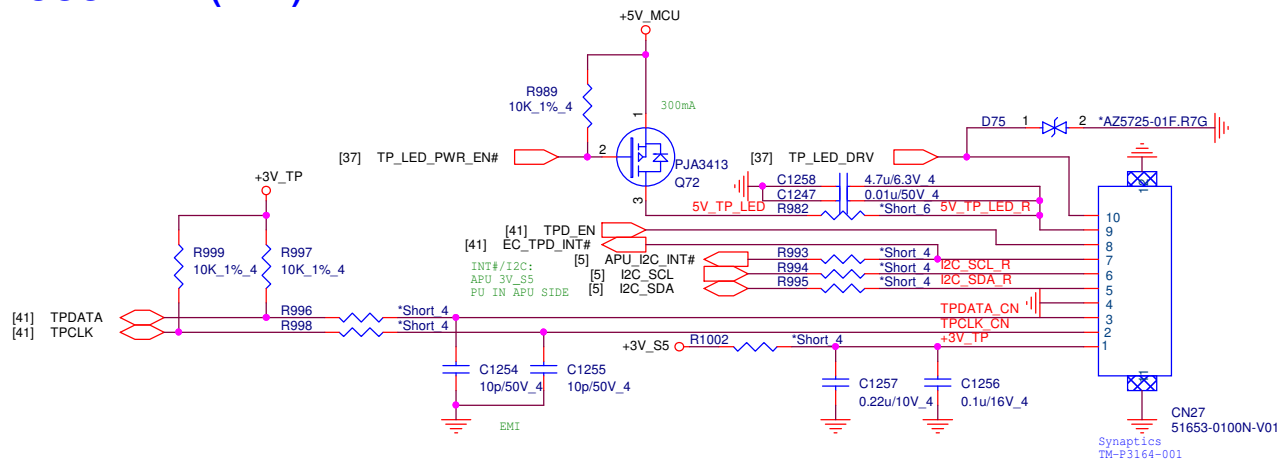
## Metal KB(KBL)



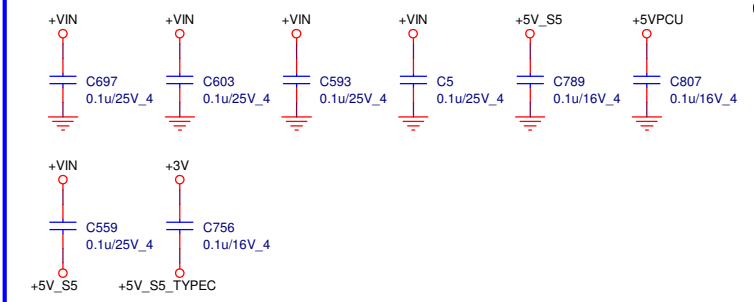
## Plastic KB(Z=5.8mm)



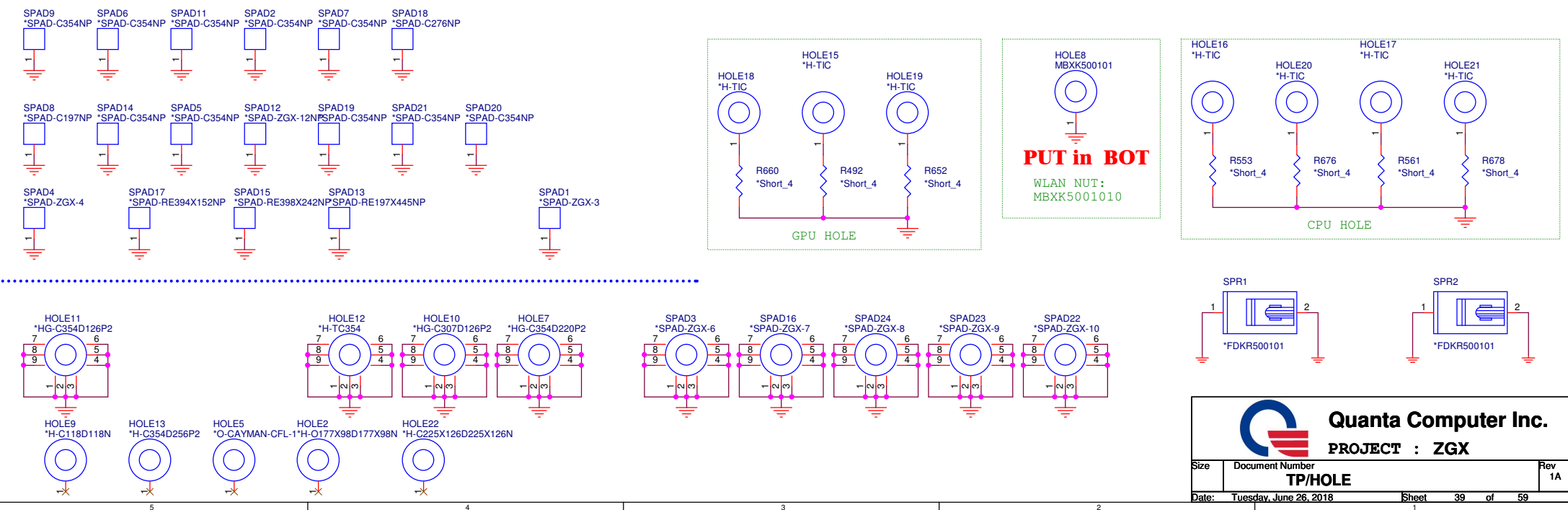
TOUCH PAD(TPD)




Stitching caps



HOLE(OTH)

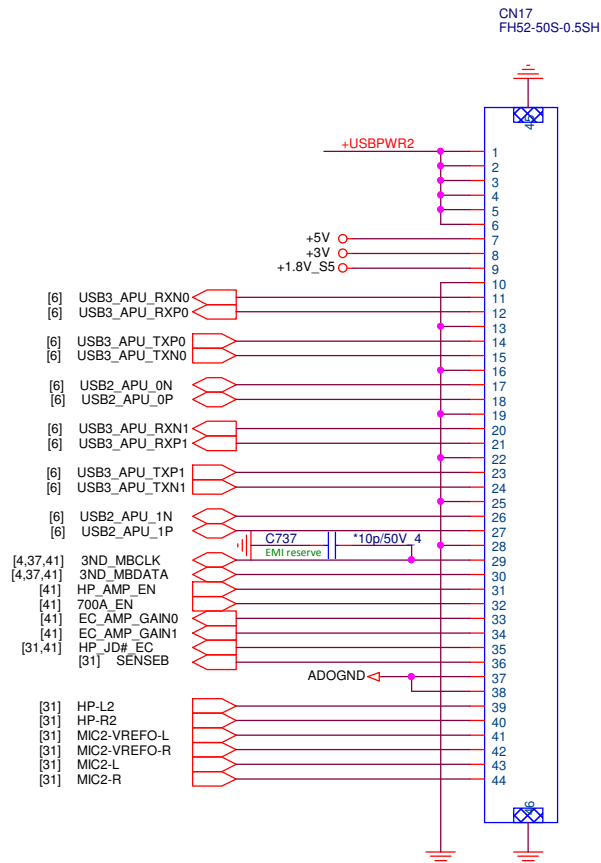
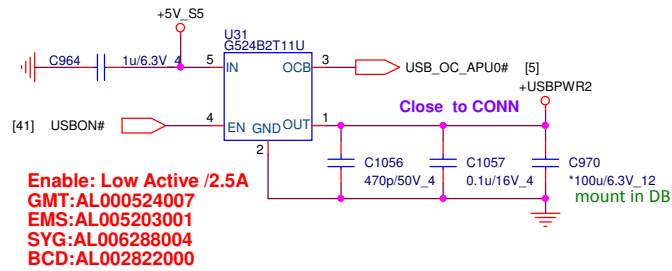




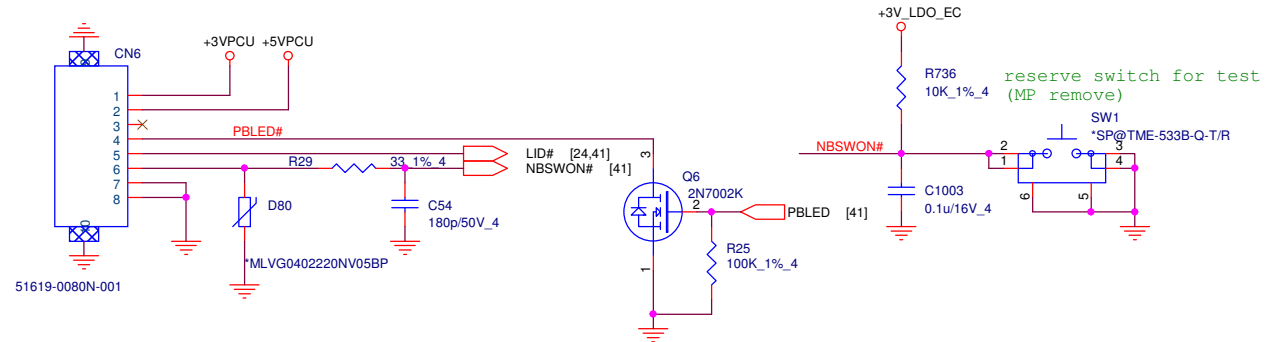
**Quanta Computer Inc.**  
PROJECT : ZGX

Size	Document Number	Rev
	TP/HOLE	1A
Date:	Tuesday, June 26, 2018	Sheet 39 of 59

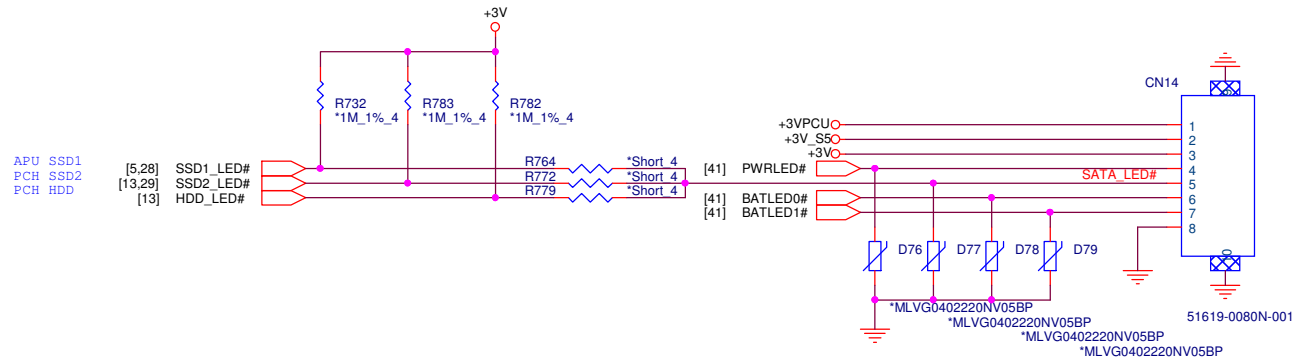
## USB BOARD (UB3)



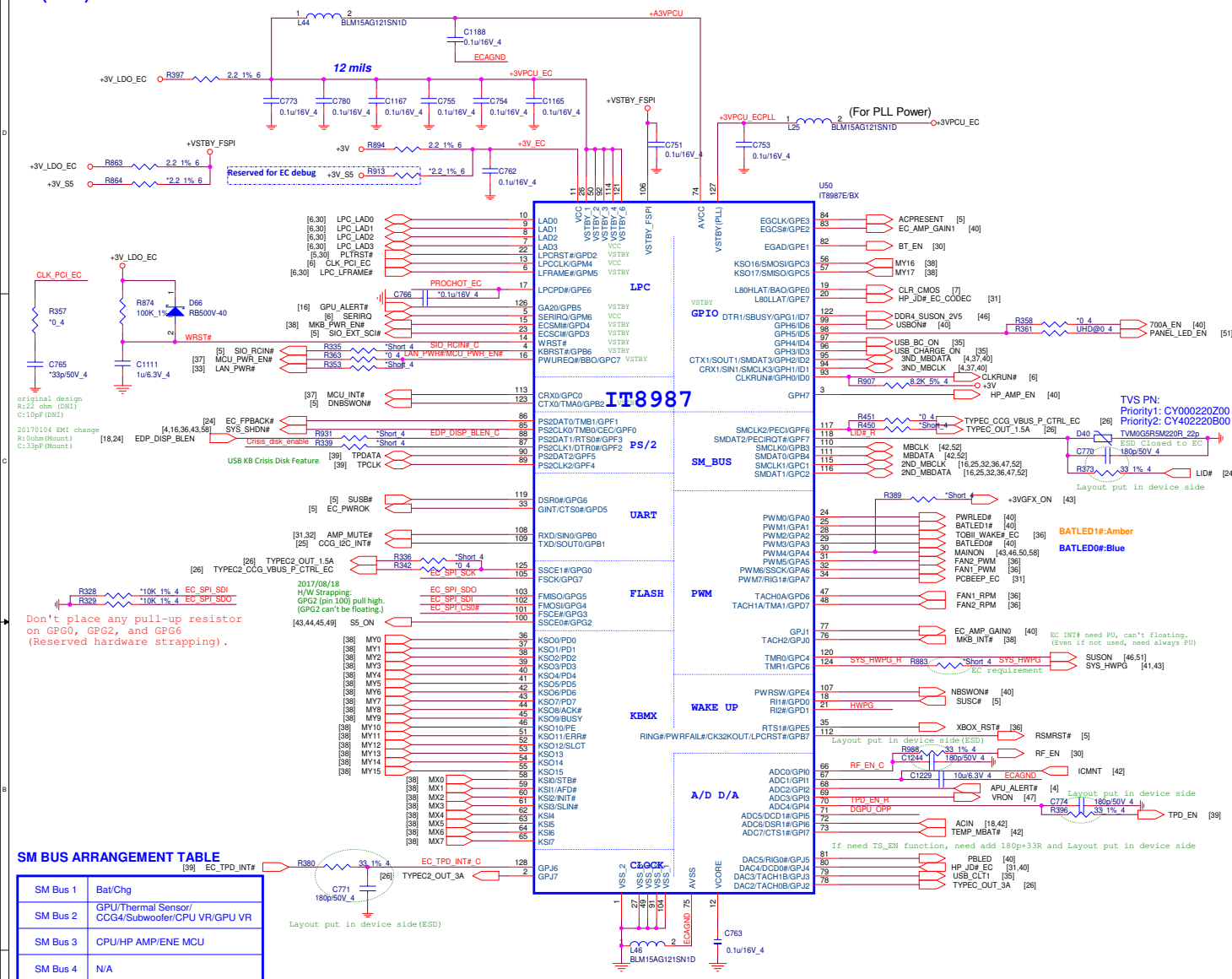
## POWER BOARD (KBC)



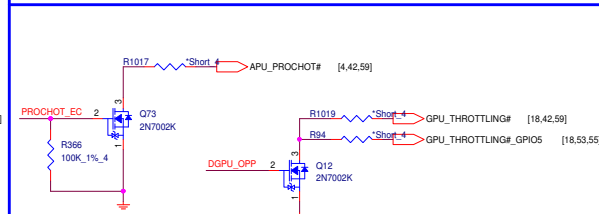
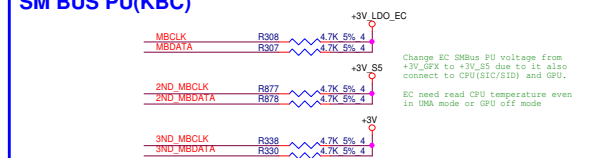
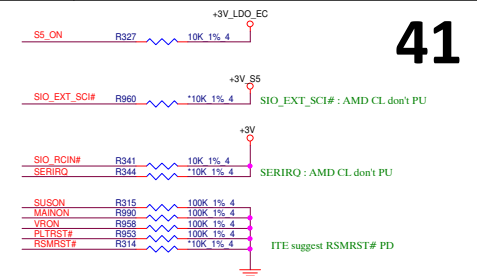
## LED BOARD(UIF)



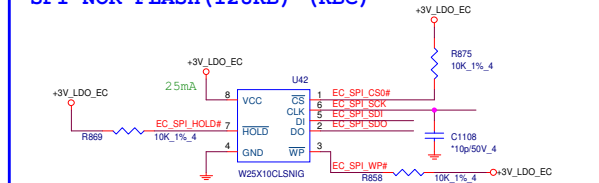




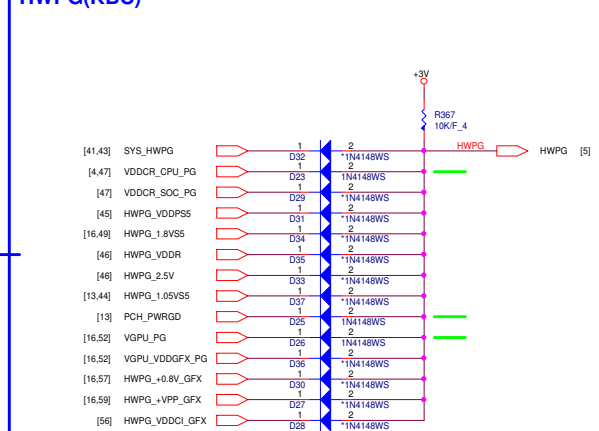
## SM BUS PU(KBC)



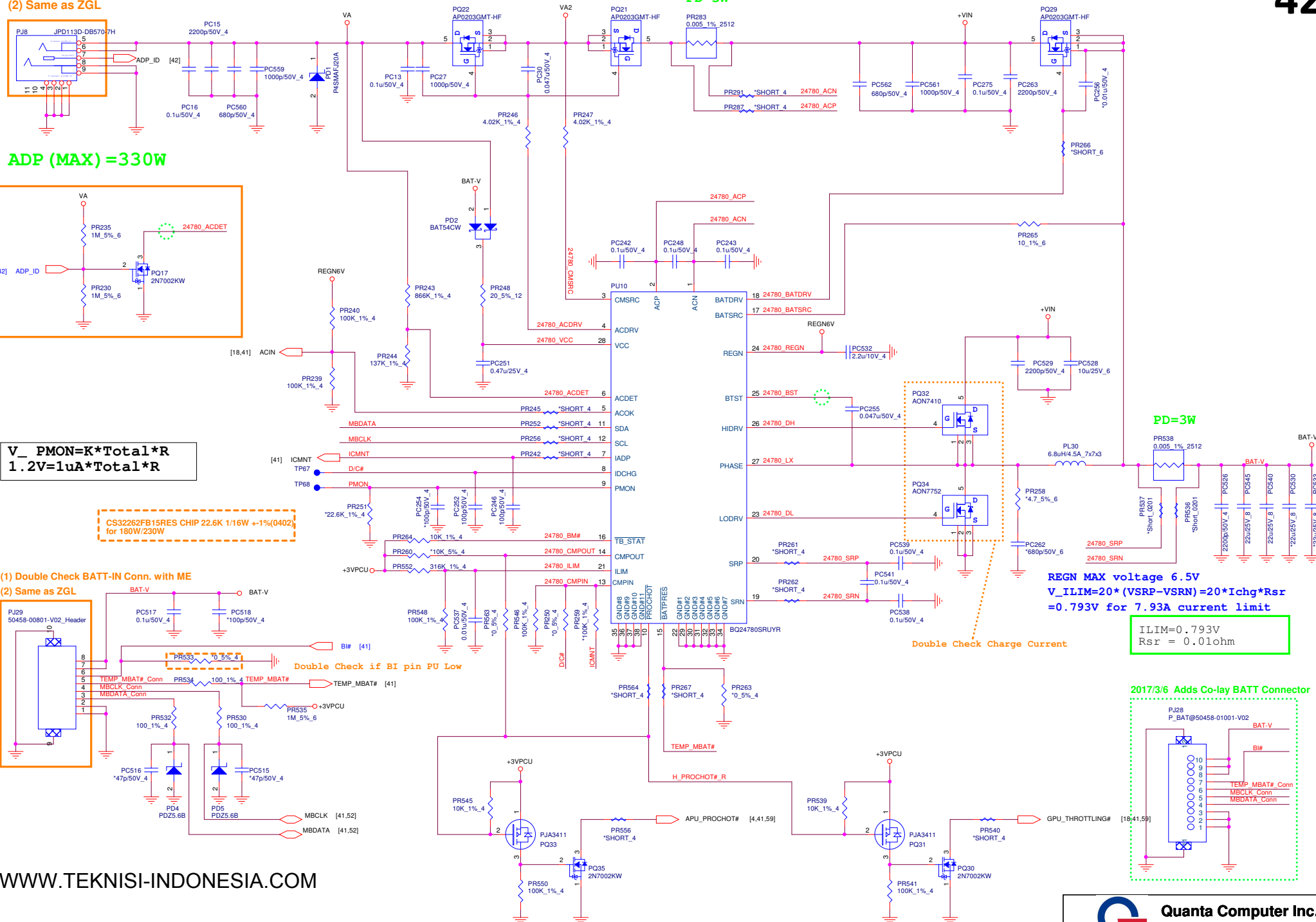
SPI NOR FLASH (128KB) (KBC)

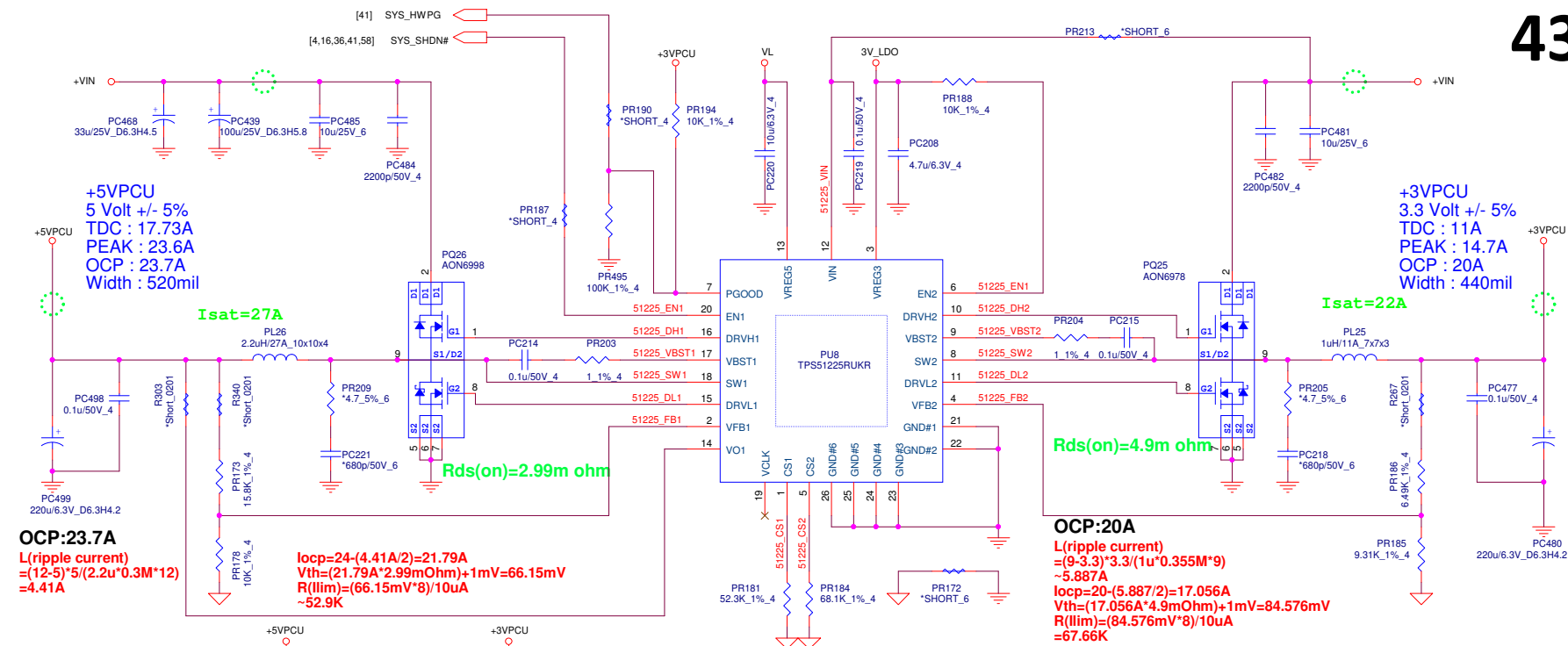


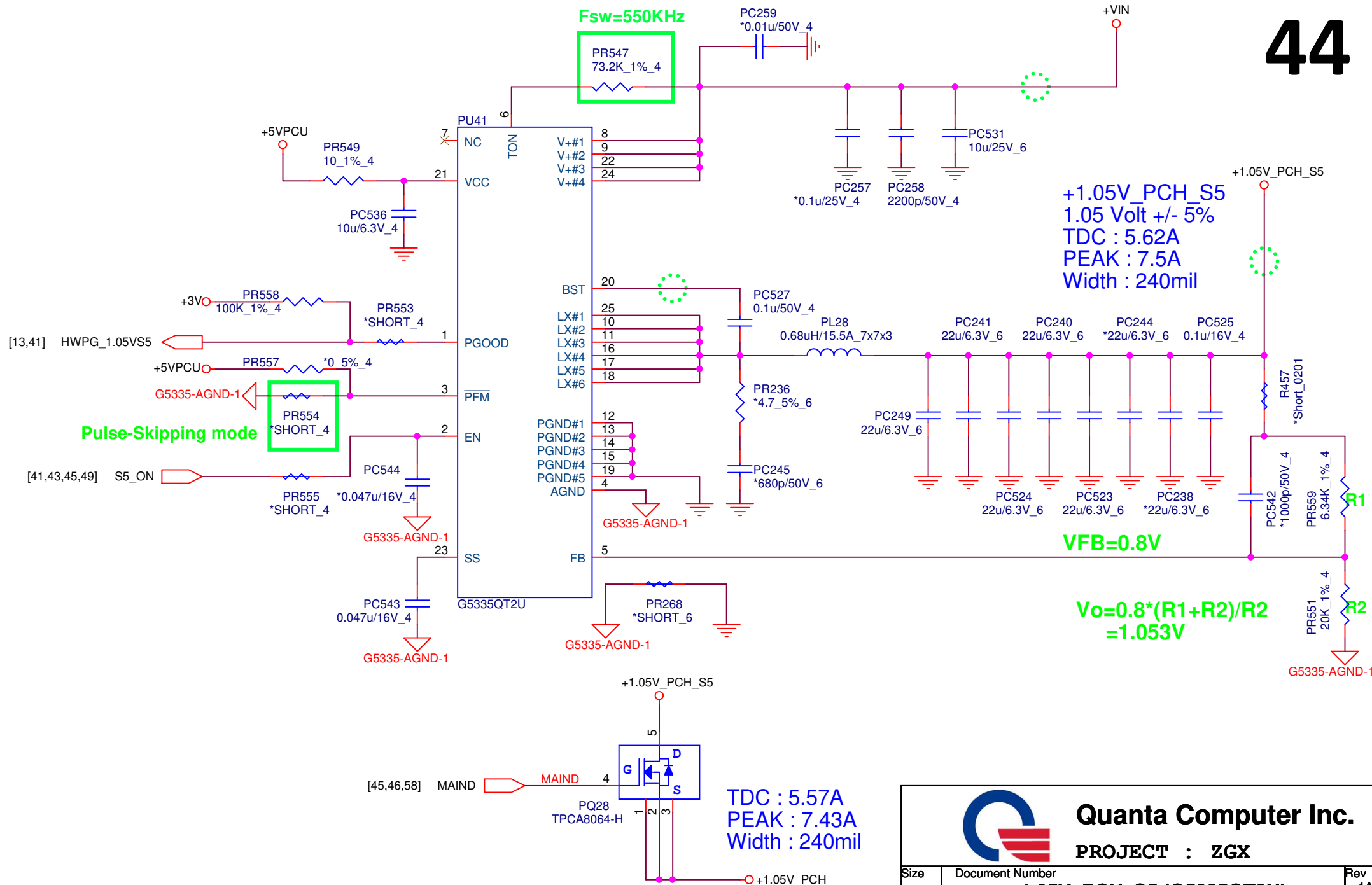
## HWPG(KBC)

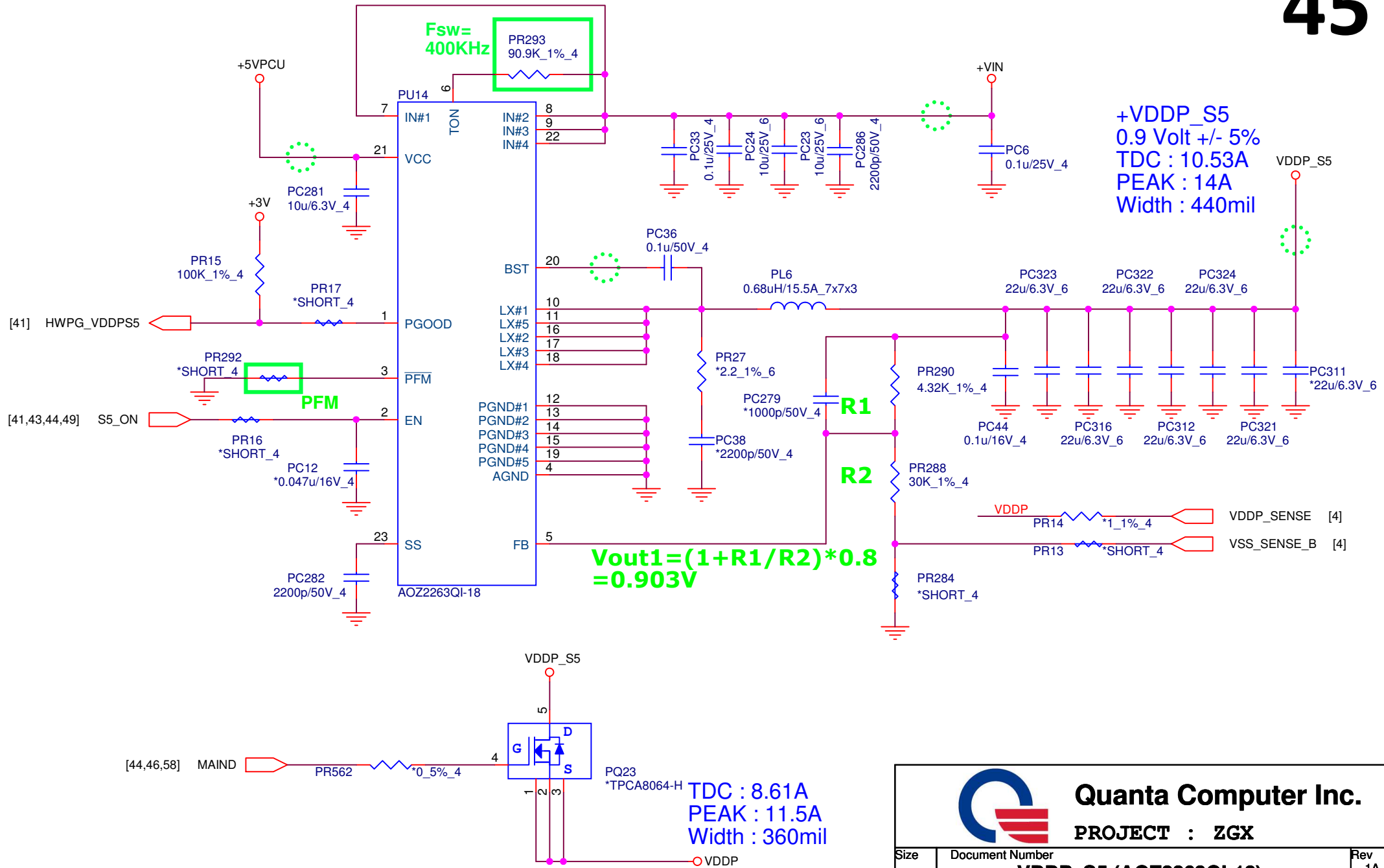


(1) Double Check ADP-IN Connector with ME  
(2) Same as ZGL





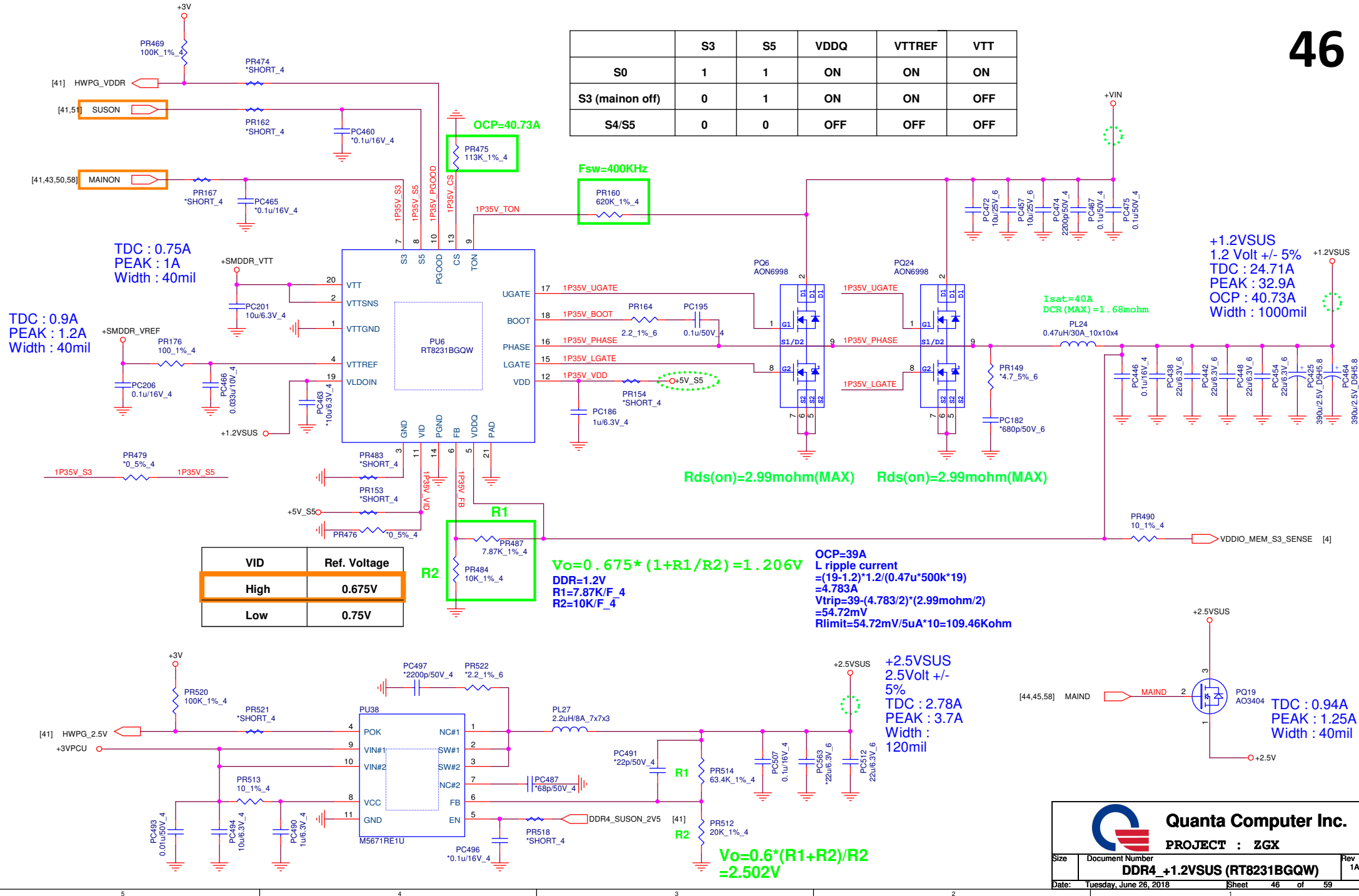




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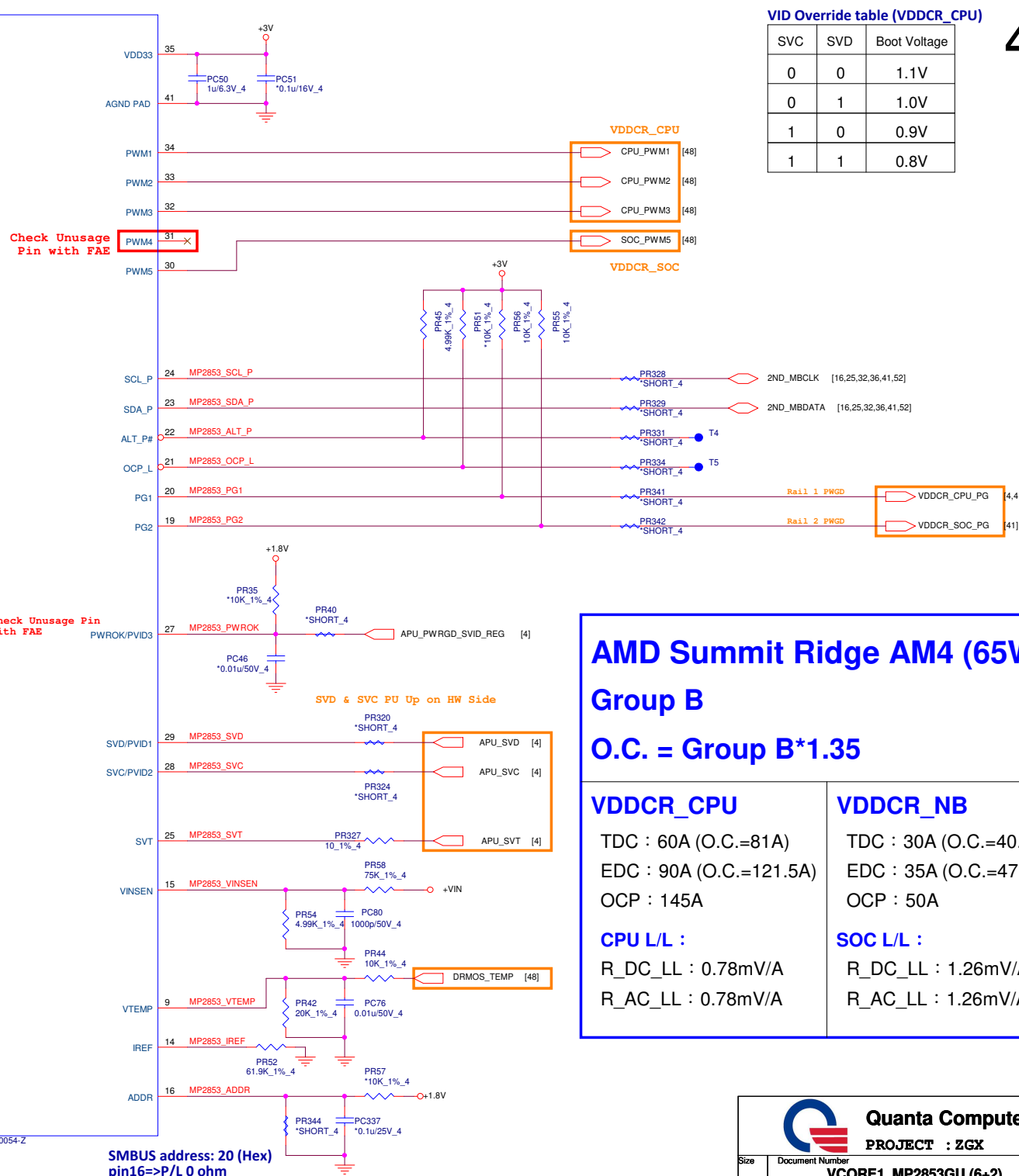
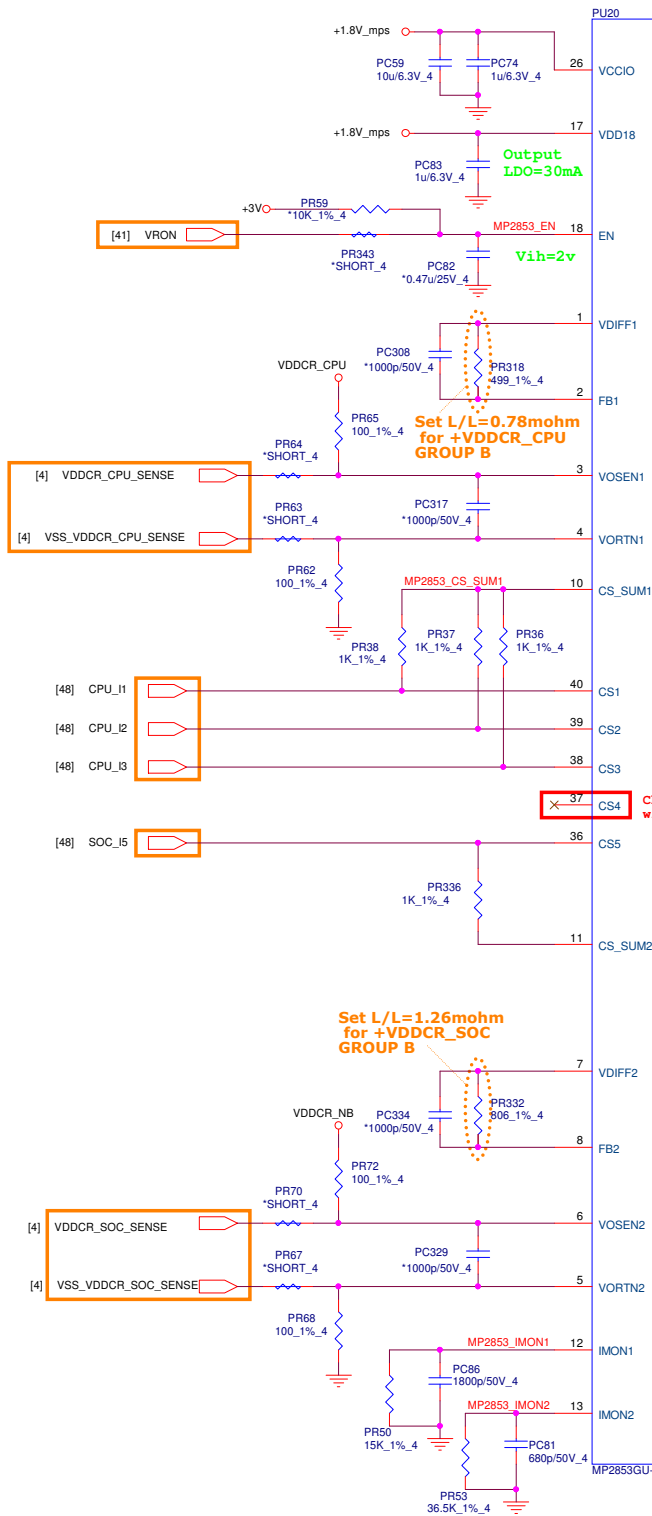
**PROJECT : ZGX**

Size	Document Number	Rev
	<b>+VDDP_S5 (AOZ2263QI-18)</b>	1A
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1	0	0.9V
1	1	0.8V



## Group B

**O.C. = Group B\*1.35**

## VDDCR CPU

TDC : 60A (O.C.=81A)

EDC : 90A (O.C.=121.5A)

OCP : 145A

## CPU L/L :

R DC LL : 0.78mV/A

R AC LL : 0.78mV/A

## VDDCR NB

TDC : 30A (O.C.=40.5A)

EDC : 35A (O.C.=47.25A)

OCP : 50A

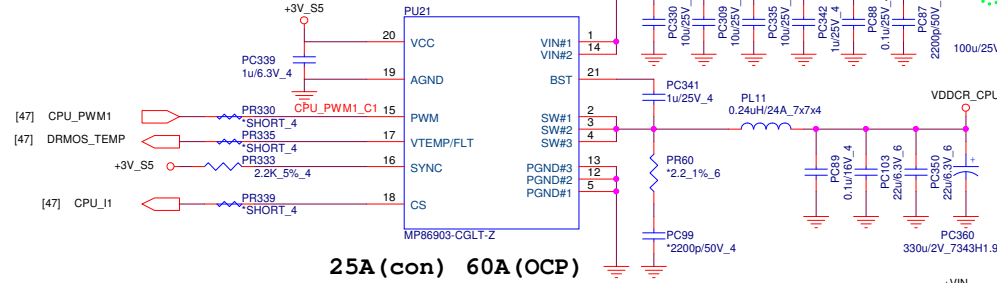
**SOC L/L :**

R DC LL : 1.26mV/A

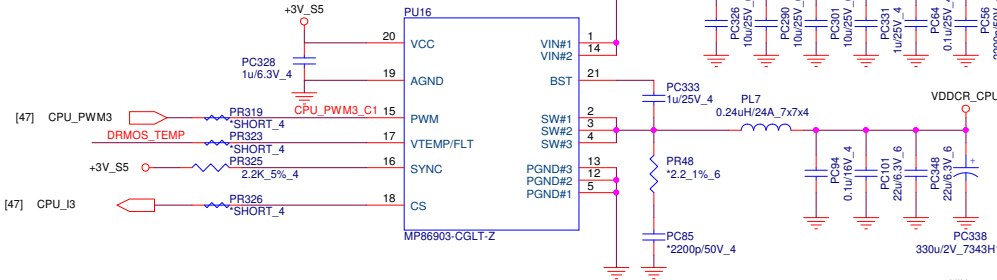
R AC LL : 1.26mV/A

# VDDCR\_CPU

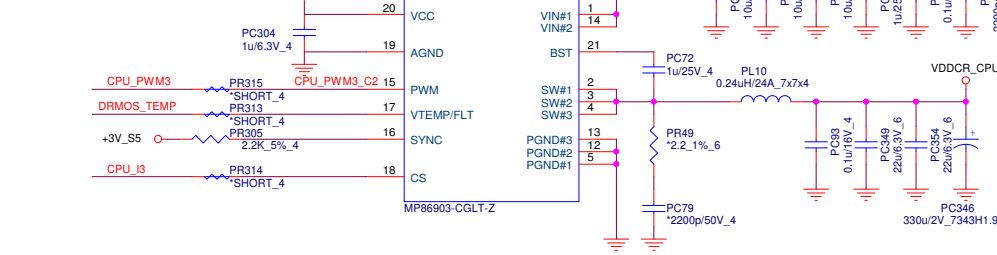
## Phase 1,2



## Phase 5,6

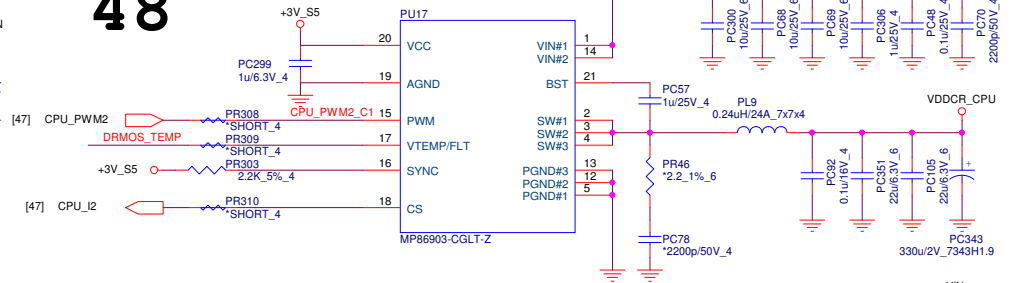


## Phase 1,2

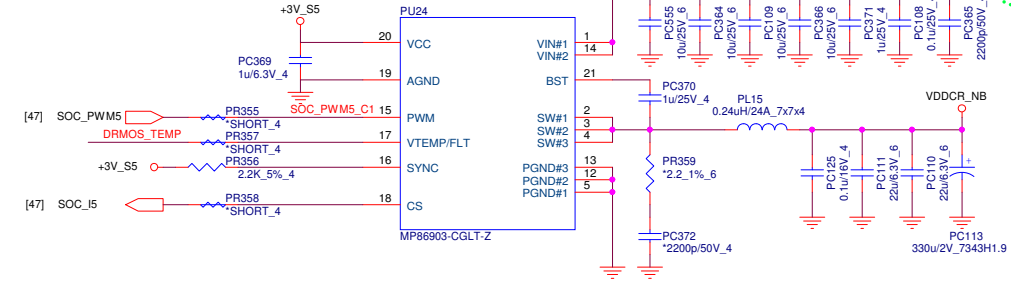


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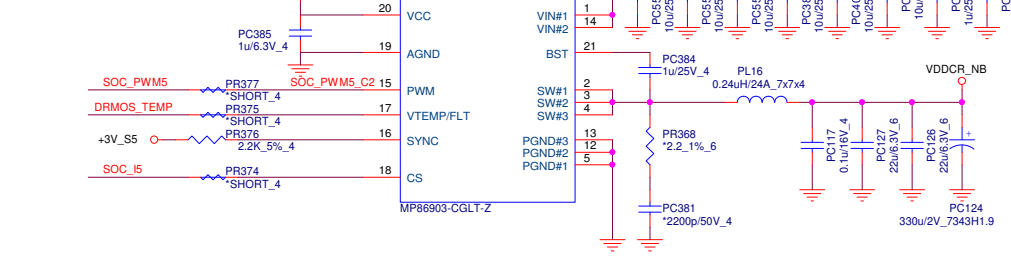
## Phase 3,4



## Phase N1,N2

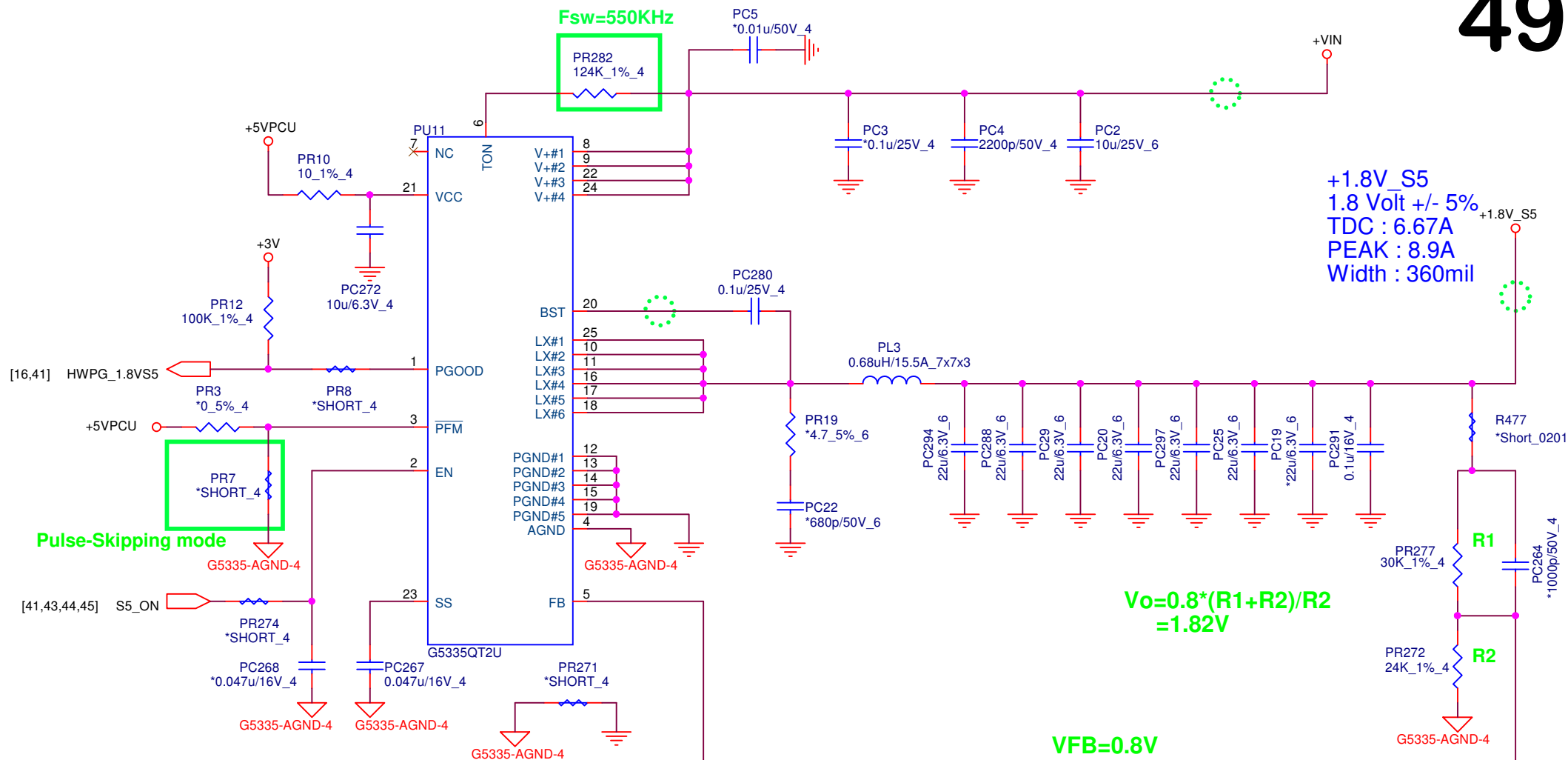


## Phase 1,2



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Size	Document Number	Rev
	VDDCR_CPU / VDDCR_NB	1A
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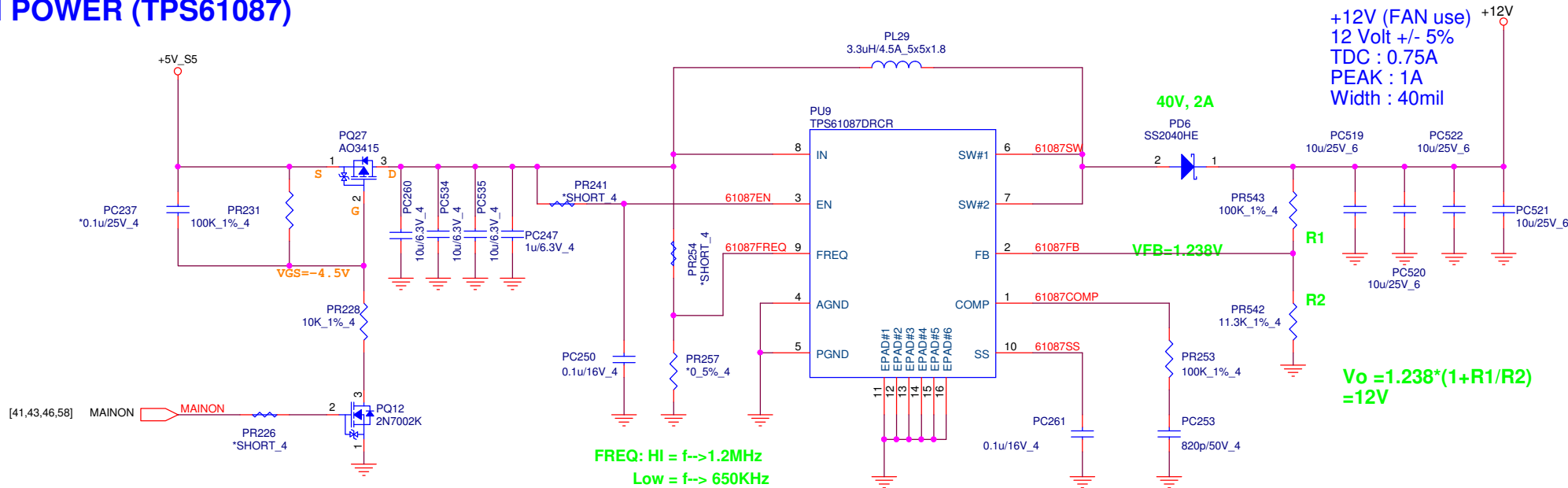
**Quanta Computer Inc.**

**PROJECT : ZGX**

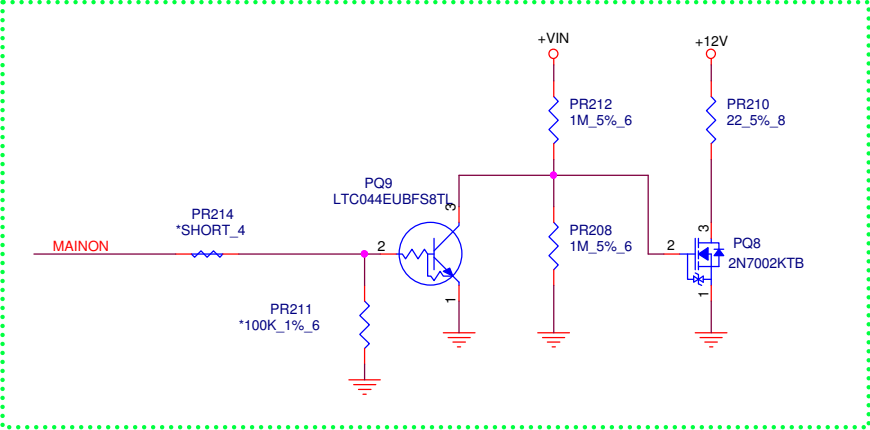
Size	Document Number	Rev
	<b>+1.8V_S5 (G5335QT2U)</b>	1A

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# FAN POWER (TPS61087)

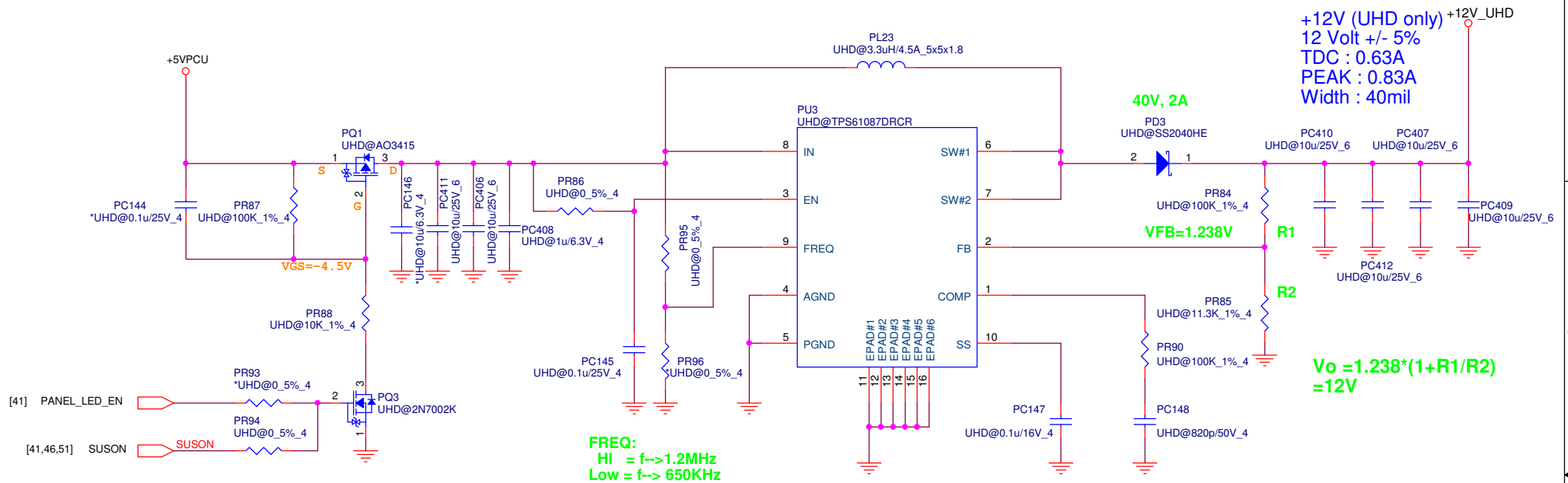


## Discharge Circuit

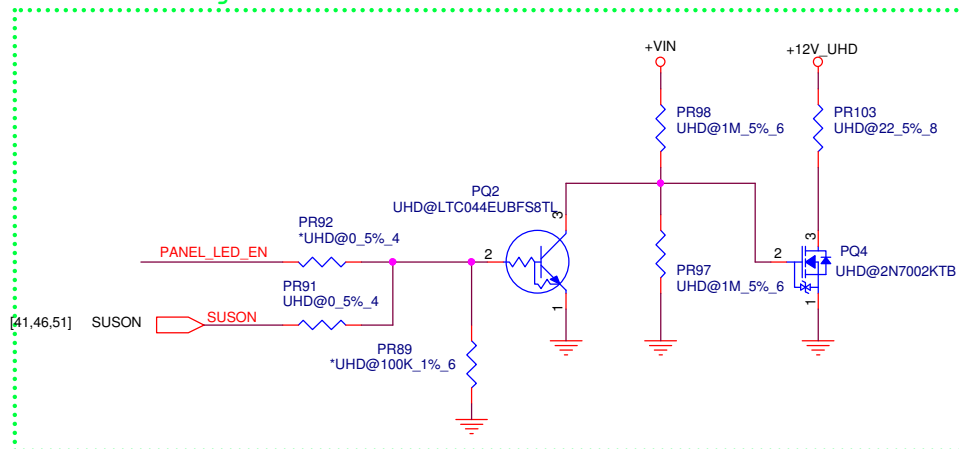


# UHD PANEL POWER (TPS61087)

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## Discharge Circuit



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**PROJECT : ZGX**

Size	Document Number	Rev
	<b>+12V_PANEL (TPS61087)</b>	1A
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# GPU Vega 10/11 (R17M-E2-90 XLM 120W)

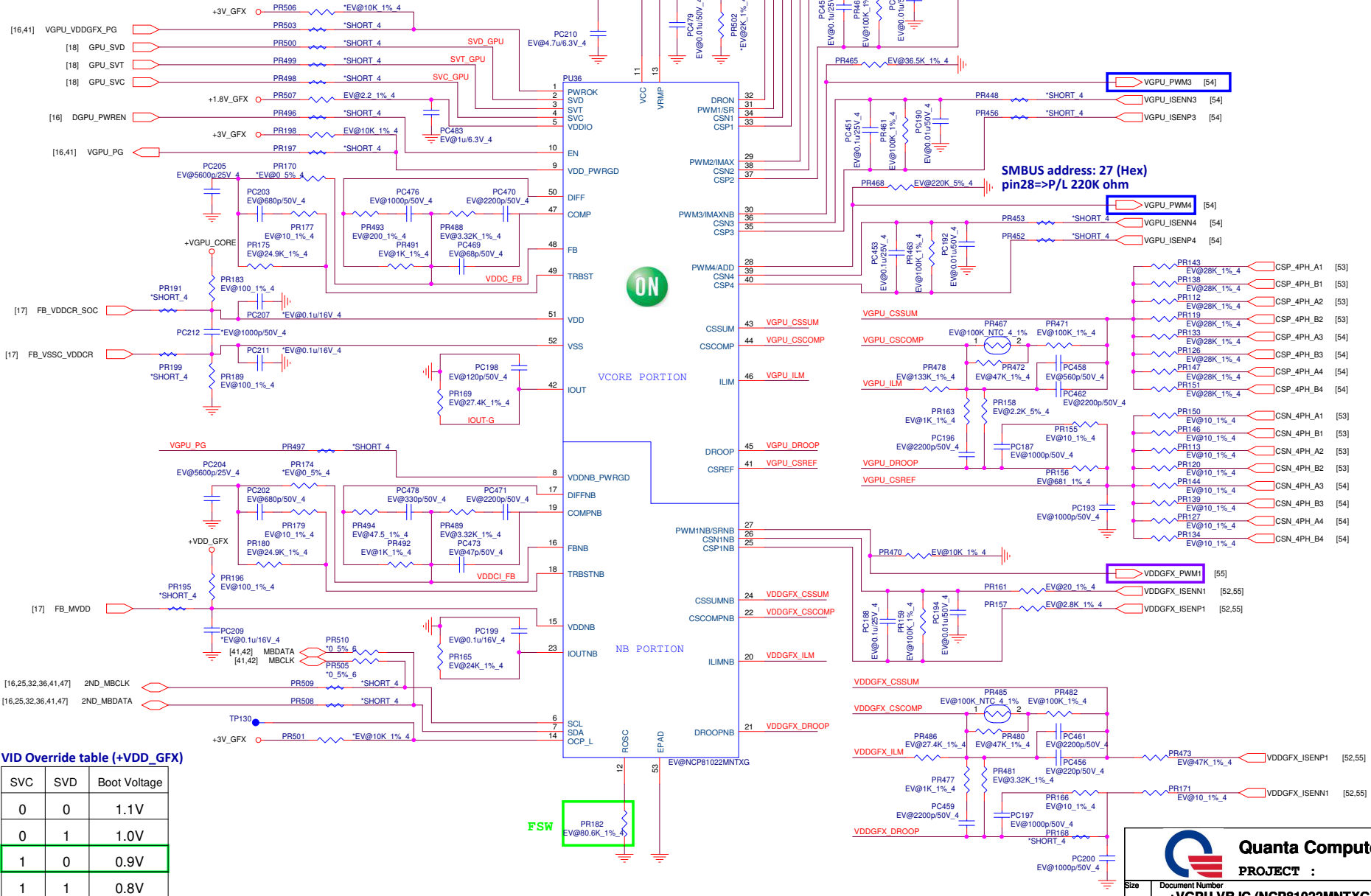
O.C. = Normal\*1.35

## +VGPU\_CORE

TDC : 140A (O.C.=189A)  
EDC : 260A (O.C.=351A)  
OCP : 470A (1.3xO.C.)  
L/L : 0.25mV/A

## +VDD\_GFX

TDC : 20A (O.C.=27A)  
EDC : 35A (O.C.=47.25A)  
OCP : 57.5A (1.2xO.C.)  
L/L : N/A

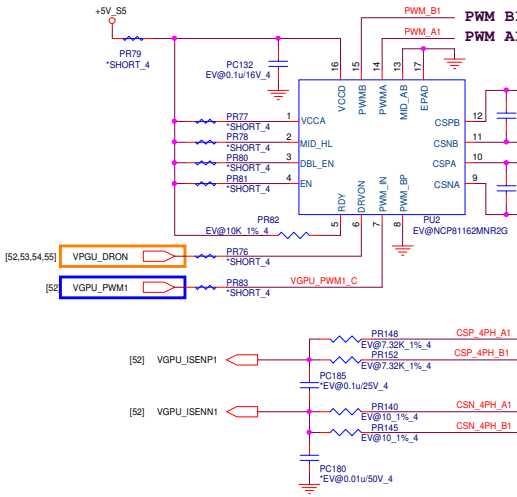


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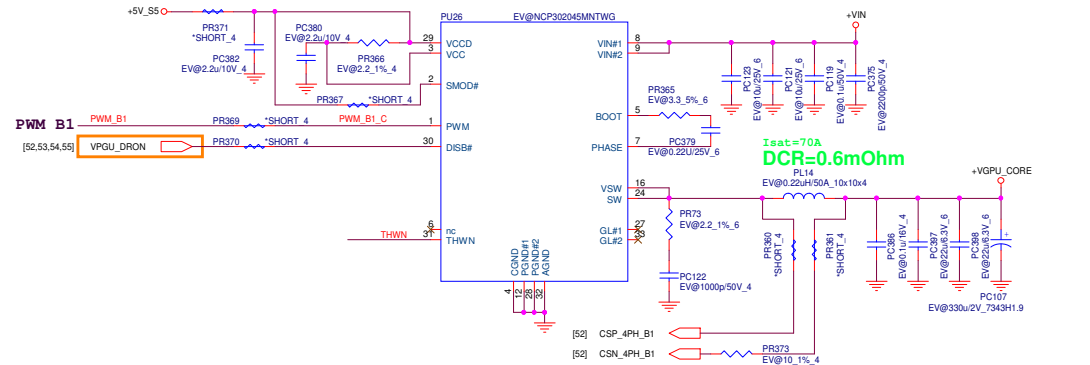


# +VGPU\_CORE

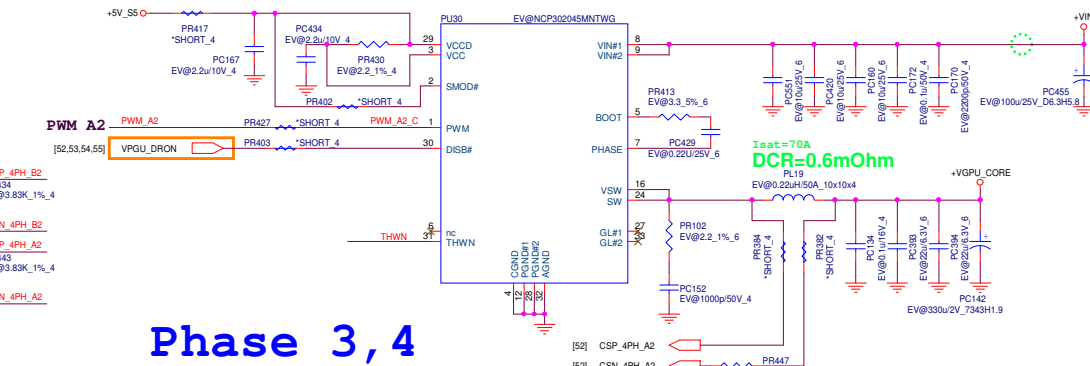
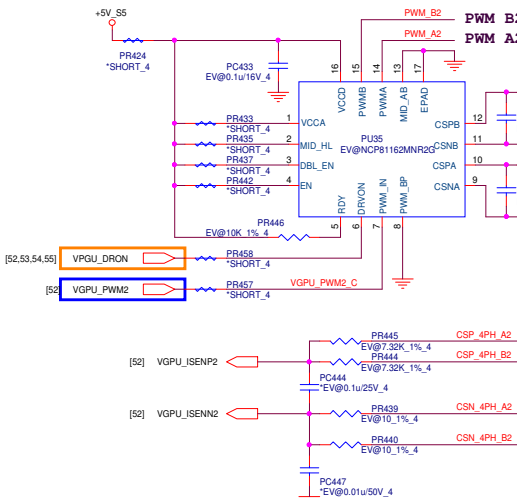
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## Phase 1, 2



## Phase 3, 4



## Phase 5, 6

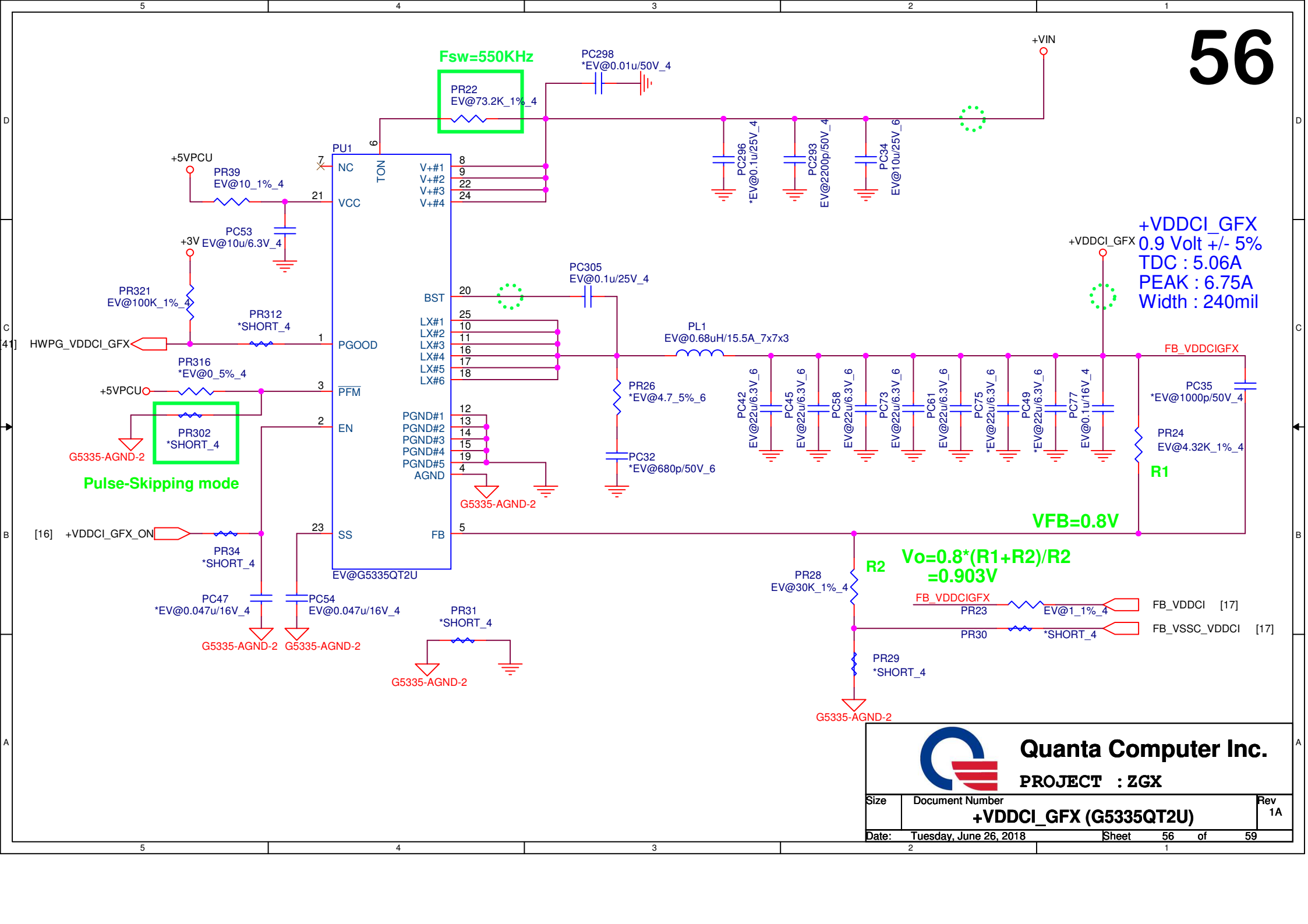
## Phase 7, 8



**PROJECT :**

Rev	
1A	

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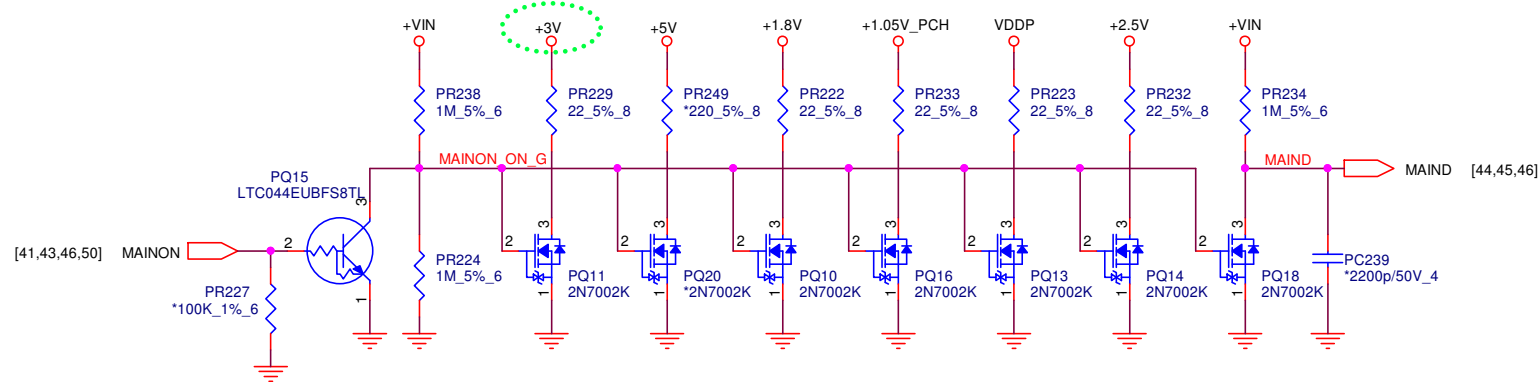
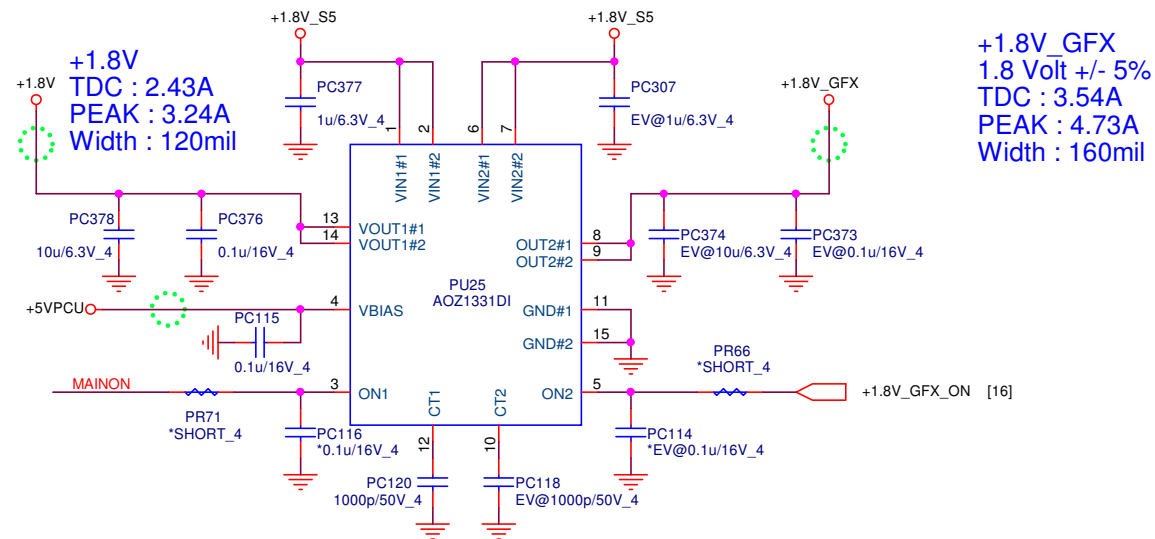


**PROJECT : ZGX**

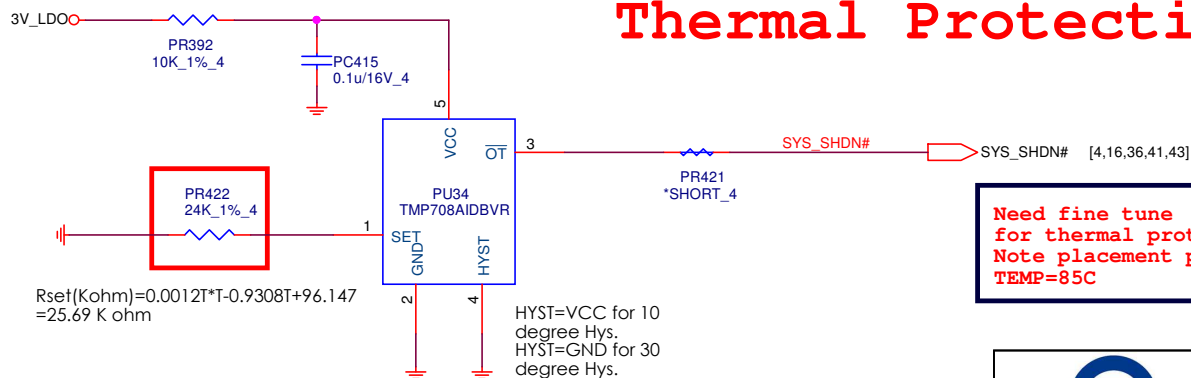
**+0.8V\_GFX (G5335QT2U)**

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## Thermal Protection



Need fine tune  
for thermal protect point  
Note placement position  
TEMP=85C



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**PROJECT : ZGX**

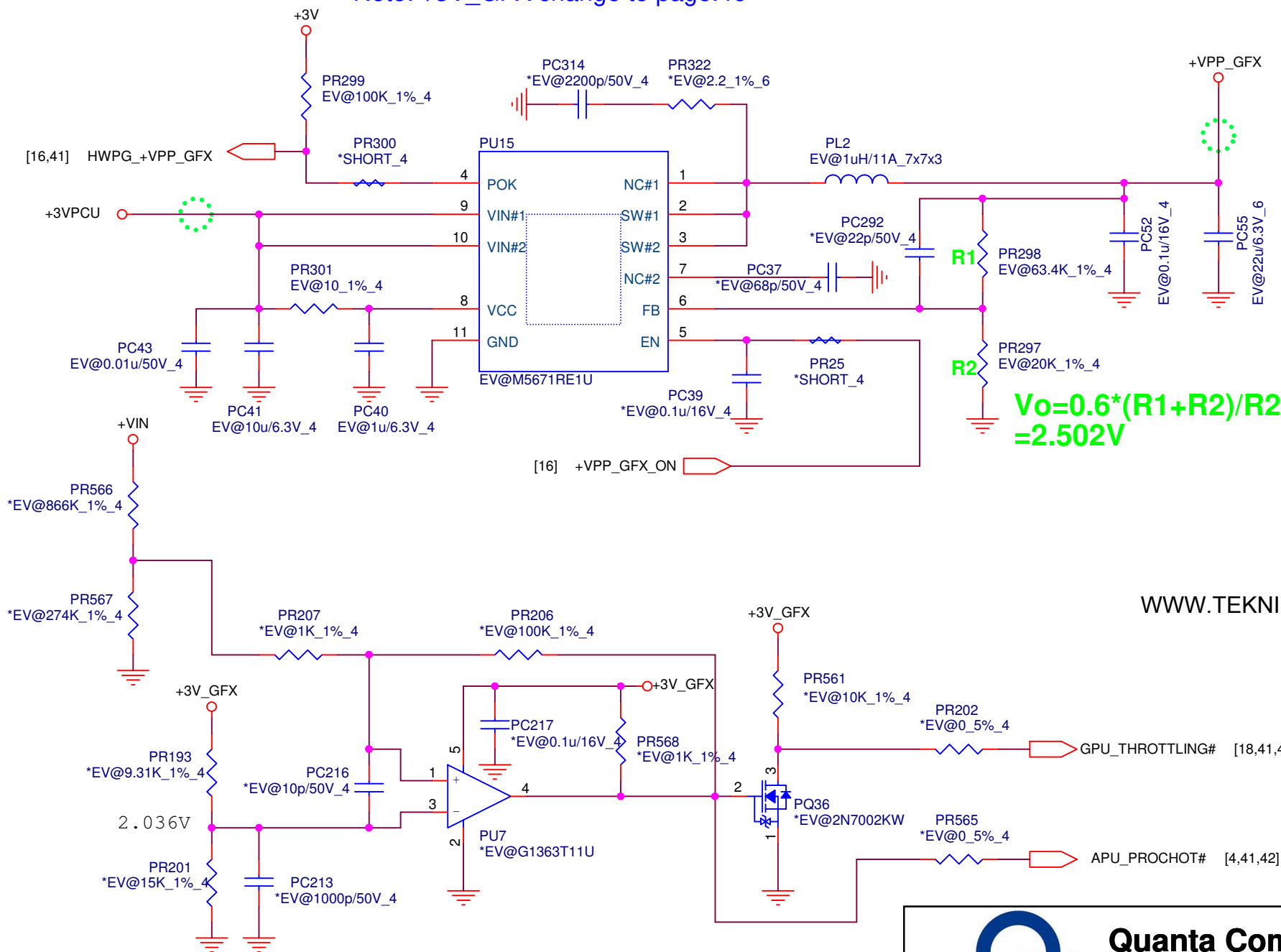
Size	Document Number	Rev
	<b>+1.8V_GFX/Thermal</b>	1A
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Note: +3V\_GFX change to page.46

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+VPP\_GFX  
2.5Volt +/- 5%  
TDC : 1.52A  
PEAK : 2.03A  
Width : 80mil



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PROJECT : ZGX

+VPP\_GFX & PCC

Size	Document Number	Rev
		1A
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